Single Crystal CdS/CdTe:P Solar Cells

by

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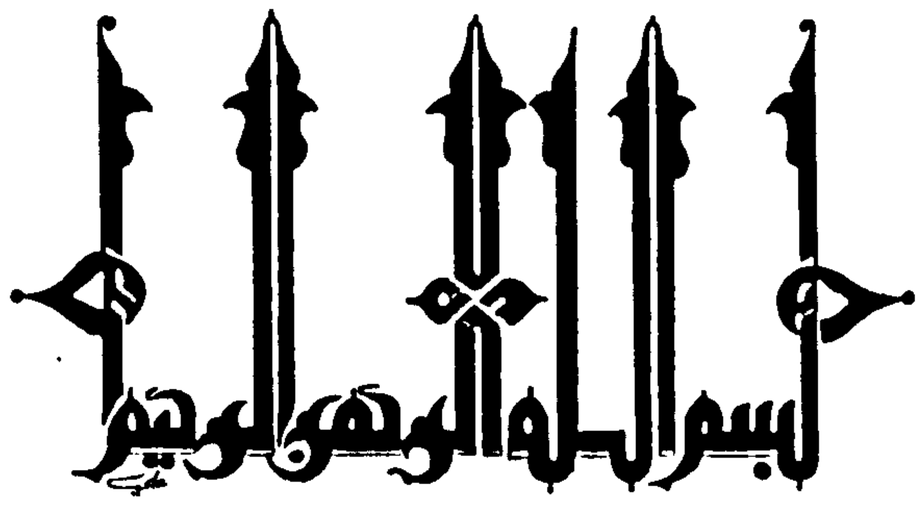

In the name of Allah,
the Beneficent, the Merciful

To my

home land

parents

lovely wife and children
(Fatima, Maean, Yaqean, Afya
and Abdelaziz)

DECLARATION

This thesis results entirely from my own work
and has not been previously offered
in any other degree or diploma.

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I ask God to help me serve my country through my field of work.

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ABSTRACT

In the fabrication of efficient CdS/CdTe heterojunction photovoltaic cells, two problems associated with the p-type CdTe have to be overcome. It is necessary to produce low resistivity p-type CdTe, and to find a good ohmic contact to it. In the first place, post-growth doping (PGD) with phosphorus was used to produce satisfactory p-type CdTe, and then several contacting materials were investigated in the search for low resistance contact.

Dice cut from bulk crystal CdTe, grown in house from the vapour phase, were treated in a saturated vapour of orthophosphoric acid in two PGD ways. The preparation methods used, the characterisation techniques and the properties of the resultant material are described in detail. PGD treatments proved capable of reducing the bulk resistivity from $10^8\Omega$cm to between 2 and 10 Ωcm, with typical carrier densities of 10^{16} cm^{-3} at room temperature. In addition to Hall and conductivity measurements, an initial evaluation of the p-type conversion was made by examining the behaviour of Schottky diodes formed using rectifying indium contacts.

CdS/CdTe heterojunctions were prepared by depositing thin layers of CdS onto the PGD treated dice using vacuum evaporation. Ohmic contacts were made to the CdS with indium, while the several materials (such as Au, Au-Cu, Au-P, Au-Sb and graphite) were investigated as contacts to the p-CdTe. The characteristics of the resultant photovoltaic cells proved to be very sensitive to the nature of the contact made to the p-type CdTe.

The series resistances of the various devices have been measured, and best results were obtained with Au-P. With an optimised cell under AM1 illumination, typical values of open circuit voltage and short circuit currents were of the order 0.74V and 22mAcm^{-2}. With fill factor of 41.7 this leads to a conversion efficiency of 9.4%. With further anticipated reduction of the series resistance, the fill factor and the efficiency should be significantly increased.

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Chapter I

Overview

1.1. Renewable Energy for A Better Tomorrow

1.1.1. World Energy Needs:

Energy is required to supply each of us with the basic human needs of food, water, and shelter, and for improving the quality of life. The demographers predict that the global population will top eight billion in 2005. Considering how world energy needs might develop in the first part of the 21st century, three factors need to be taken into account; a) the world population, b) the standard of living (GNP per person) and c) the efficiency of energy use (energy requirement per unit of GNP).

a) The world population is growing more rapidly now than at any time in history and is expected to almost double over the next 40 to 60 years.

b) To improve the standard of living the economics of the world must grow steadily in both the developed and developing world. This will depend critically on energy availability. The wealthy developed world standard of living is increasing steadily, while pressure continues for better conditions and economic growth in developing countries. An abundant supply of affordable energy is needed to meet these requirements.

c) the effectiveness of energy conservation is another main factor in controlling energy waste. It is influenced, to some extent, by the relative contribution of the manufacturing and service sectors to the economy and climate.

The product of the second and third factors is the energy consumption per person. As one might expect, this shows substantial variations around the world. On

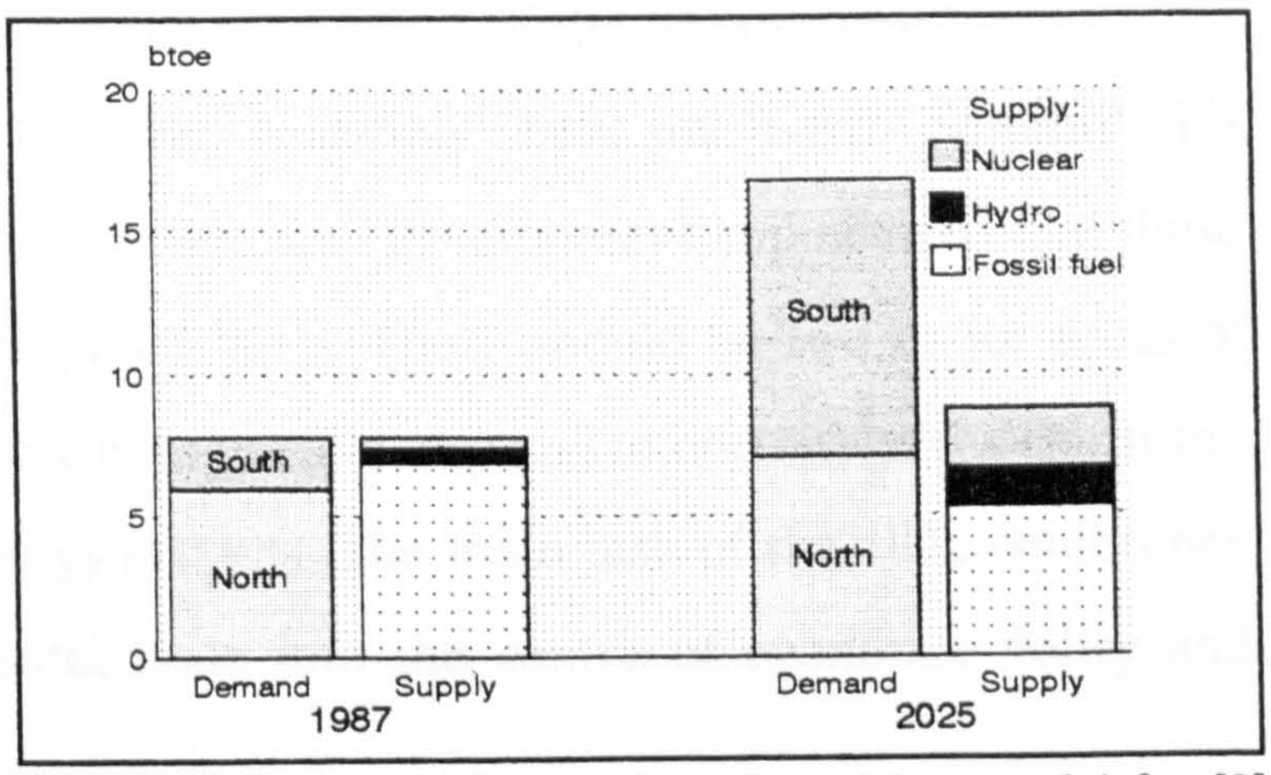

Figure 1.1 .. World Energy Supply and Demand (after[2] p.35)

average each person in the developed world - the so called north - uses about 5 tonnes of oil equivalent each year; in the south - the developing world - consumption is only one tenth of that. The world total is about 8 billion tonnes of oil equivalent per year, with a quarter of the world population in the developed world using three-quarters of the energy. Figure 1.1 shows the current and future demand and supply of energy [1]. It shows also that there will be a substantial shortfall if the economics of the south is to expand at even the present low level.

1.1.2. Environmental Issues:

The atmosphere is the principle medium through which human activity is interacting to shape the conditions on which the future of life on the planet depends. Our behaviour has now reached a level at which it is affecting the balancing systems that produce the conditions that make life on earth possible. The world is becoming increasingly conscious of the damage to global environmental systems (such as the greenhouse effect and ozone depletion) caused by the production and consumption of energy.

The Scientific Working Group of the Intergovernmental Panel on Climate Change (IPCC) has estimated that emissions from energy-related activity contributed about half of the warming effect of human activities during the decade from 1980 to 1990, and emissions due to fossil fuel combustion into the atmosphere amount to about 70-90% of the greenhouse effect [1]. Changes in

energy policy are thus crucial for the protection of the atmosphere.

The 'United Nation General Assembly' held an 'Earth Summit' this year to discuss the issue of environment and development and advised that these must be dealt with on an integrated basis. There should be two major areas of activity; programmes to increase energy efficiency and to encourage the transition to environmentally sound energy systems. The main task of the 1992 conference was to move the environmental issue into the centre of economic policy and decision making.

The issue of power generation and the environment has been discussed in depth at many international conferences, see for instance reference [2]. This topic was addressed for nuclear [3], coal [4], diesel and gas engines [5] and geothermal [6] power sources and practical solutions were suggested in many other reports [see, 7]. The threats to the environment associated with such power sources can only combated by collaborative action which should begin immediately before the scientific evidence ultimately becomes definitive. On an issue like this that affects the fate of the entire human community we simply cannot afford to take the chance of waiting too long. Changes in industrial processes will be difficult, but they are also feasible. Our common future on this 'Only One Earth' is in a very real sense 'in our hands'.

1.1.3. Energy Supplies

Nearly 90% of the world's needs are currently supplied by fossil fuel; the remainder almost entirely by hydro electric power and nuclear energy. Conventional fossil fuels such as coal, oil and gas are finite and will run out in the foreseeable future since these fuels are being consumed much faster than they are being produced. Geological formation of these fuels takes 600 million years while modern rates of consumption are measurable in centuries. The well known disasters at Chernobyl and Three Mile Island speak for themselves on how

disastrous the use of nuclear energy can be. Therefore, some form of renewable energy source, other than hydro-electric, has to be developed on a large scale.

1.1.4. Solar Energy and Economical Views

To reduce the dependence of energy on oil, R&D on various alternative energy resources has been advanced in recent years. Such energy resources are divided into two categories, i.e. renewable and non-renewable. Among the former, photovoltaic (PV) generation systems can be manufactured commercially. To appreciate the quantity of solar energy available, it is found that on a bright summer day at noon the solar energy falling of the earth's surface is about 1000 watts per square metre. Full conversion of such an amount for a single square metre into electricity would power ten 100W bulbs, or two motors, or several 25 inch television sets [8].

Light is absorbed in a solid by transfer of the photon energy into excitation of electrons. If the electrons and holes generated by this photo-excitation are separated by an internal electric field and subsequently collected, then both a photovoltage and a photocurrent are produced. The photocurrent is a result of minority carrier transport and is thus a reverse current, whilst the photovoltage is positive. The device operates in the fourth quadrant of the diode I/V diagram and is a power generator. Photovoltaic modules, whether single crystal, amorphous silicon, or concentrators, are built up electrically from individual cells. Cells are small, ranging up to several cms across, and produce typical output voltages of between 0.5 and 0.8 V and 20 to 30 milliamperes per square centimetre. They are wired in series to provide greater voltage and in parallel to provide greater current. An entire plant might contain millions of cells. Large scale photovoltaic power generation of the future will require high efficiency, large area, low cost PV modules manufactured by techniques that are adaptable to large volume production.

Forty years ago, PV cells were being researched in the laboratory. With technological improvements, PV found its first commercial use in space; as costs declined terrestrial applications became economical. Many feel that the ultimate application of PV will be its use for bulk power generation. Achieving this is still too expensive for most utility applications. Nevertheless, use of renewable and energy efficiency measures will, in the long run, produce savings. Photovoltaic (PV) power systems are widely used in remote locations because of their high reliability and low operating costs. For example ,PV is in wide use by at least one utility for corrosion protection, data acquisition, radio repeaters and similar low power applications. Because of their high initial cost, however, these systems have not been widely utilised as grid-connected sources (for example in the U.S.A. 219 systems are known to have been installed between 1978 till 1990, and none have been grid-connected yet) [9]. A bibliography of utility-interactive photovoltaic generation up to 1988 is given in [10].

It is expected that the market for solar cells will expand rapidly as the cost of power from conventional and non-renewable sources rises, while that of solar cells should fall in real terms because of technological improvements and economies of large scale manufacture. Figures 1.2 and 1.3 show the improvements in conversion

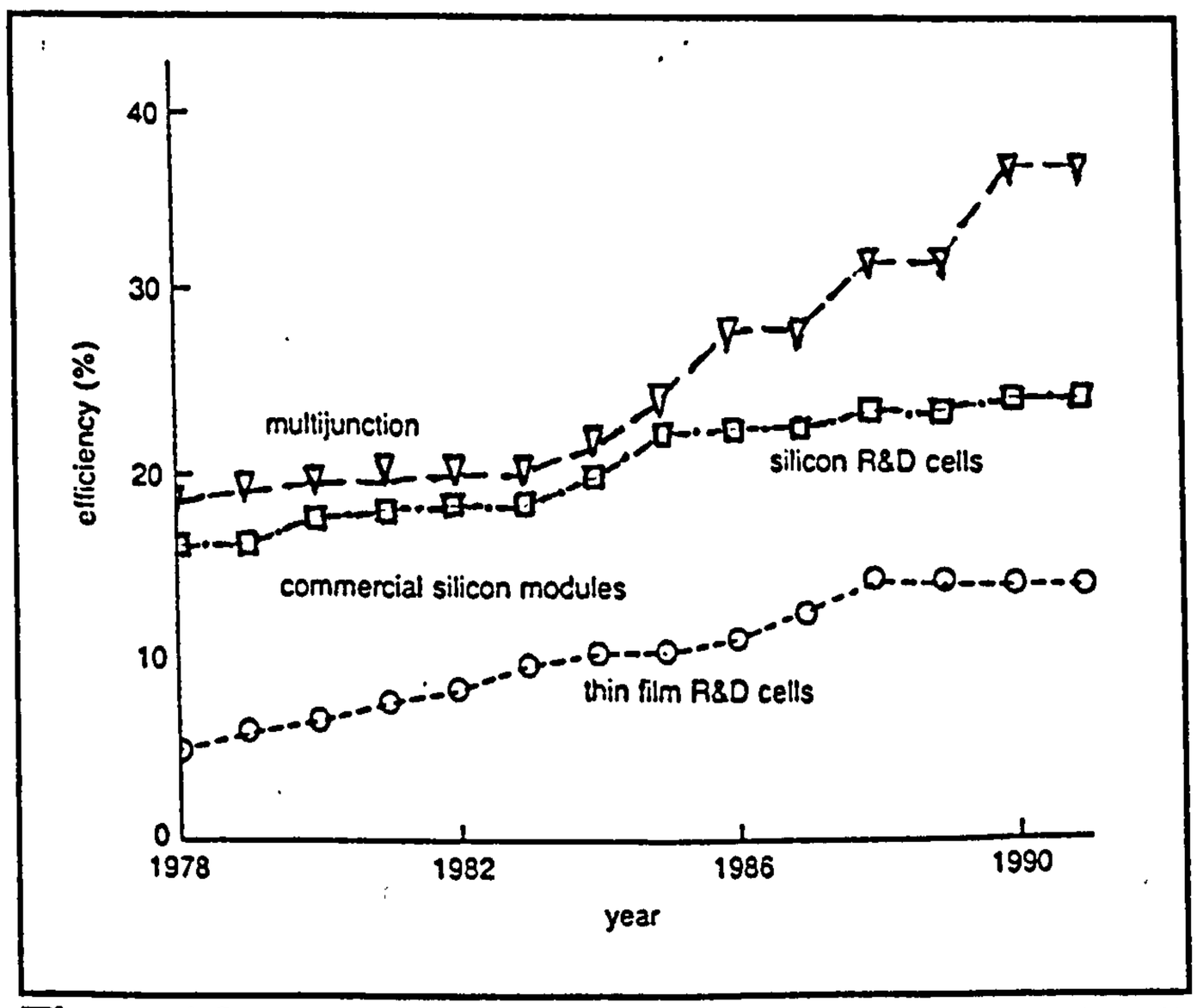

Figure 1.2 .. Improvement in conversion efficiency of cells and modules since 1978. (after[11])

efficiency and the reduction in module cost achieved to date [11]. It is clear that the price of photovoltaic energy continues to decline. For example in 1956 silicon single crystal homojunction cells cost 350$ per peak watt (W_p). By 1966 the cost had dropped to 100$ W_p through improved processing and technology [12], and by 1977 it was around 15-25$ W_p for arrays. The production of polycrystalline silicon cells in the USA increased by one third from 1984 to 1985 (from 1.8 to 2.4 MW), while production of single crystal photovoltaic cells dropped by 19% (from 6.6 to 3.35 MW). On the other hand, work on amorphous silicon photovoltaics is expanding at a fast rate [13]. By the year 2000, the USA photovoltaic program aims to reduce the price of photovoltaic energy to 0.1 to 0.3$ W_p [14].

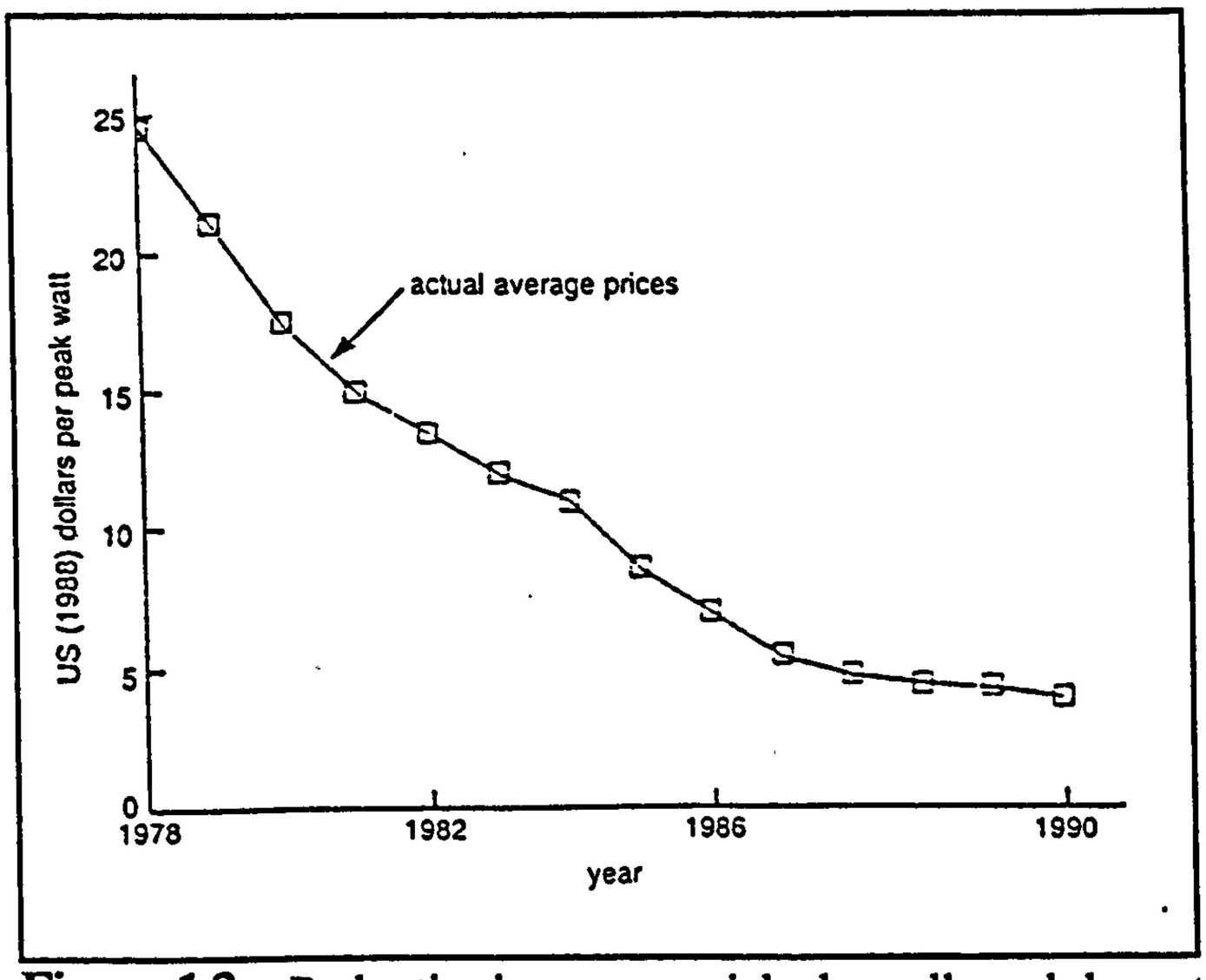

Figure 1.3 .. Reduction in commercial solar cell module cost for large orders since 1978. (after[11])

1.2. History of Photovoltaic Power

The fundamental conversion of light to electricity takes place via the photovoltaic effect, discovered by Edmund Becquerel in 1839 who observed a light-dependent voltage between two metal electrodes placed in an electrolyte solution [15]. A similar effect was observed by Adams and Day [16] in 1877, shortly after the discovery of photoconductivity in selenium by Smith [17] in 1873.

Fritts [18] produced a selenium cell with a transparent gold counter-electrode and confirmed the existence of an E.M.F which was first reported by Adams and Day. Minchin [19] developed the first thin film cell by oxidizing chemically a tin foil to give a tin-tin oxide cell. Many of the subsequent solid state workers including Hallwachs [20], Lange [21], Schottky [22] and Grondahl [23] prepared photovoltaic cells on selenium and cuprous oxide.

Thereafter a variety of materials and devices were investigated, but it was not until 1954 that work directed towards the fabrication of devices utilizing the photovoltaic effect was reported in the literature. In that year, Reynolds et al [24] obtained about 6% conversion efficiency with a Cu_2S-CdS p-n heterojunction and Chapin et al [25] reported a 6% efficiency for a diffused silicon p-n homojunction. With these pioneer studies, the foundation was laid for the further development of a photovoltaic device technology. Developed at Bell Laboratories, the first utilization of photovoltaic cells (homojunction silicon cells) saw their application on Vanguard I, a U.S. satellite launched in 1958. The Vanguard I cells were made by hand and cost over 1000$ per watt [26].

For the last 23 years a considerable volume of research has been directed toward terrestrial photovoltaic conversion of solar energy. Continued effort to fabricate high efficiency solar cells has succeeded in producing single crystal Si and GaAs solar cells with efficiencies in excess of 23% [27] and 24% [28], respectively. However, the high cost of GaAs and Si single crystals make these cells too expensive for wide terrestrial applications. An updated review of the status of solar cell applications has been given by H.Moller [29]. A major objective has been to lower the manufacturing cost of cells, and one obvious solution was the use of thin film devices with a creditable efficiency goal of at least 10%. At present four types of cells have reached this value in laboratory samples of small area of about 1 cm^2. Apart from one based on amorphous silicon (α-Si), the others involved II-VI semiconductor compounds. The devices being

studied most intensively are; heterojunctions based (i) on $CuInSe_2$ using CdS or $Cd_{0.8}Zn_{0.2}S$windows and (ii) on CdTe coupled with CdS or ITO.

1.3. Advances in Solar Cells

During the last decade the photovoltaic field has witnessed several technical breakthroughs which resulted in the demonstration of cost-effective processing techniques and solar cells with conversion efficiencies approaching 15%. However, an additional challenge has to be met before photovoltaics can be a widely used as a source of electrical power. Among many materials that have been evaluated for solar cell applications, cadmium telluride and copper indium diselenide have clearly emerged as the most promising semiconductors to be used in the fabrication of high-efficiency polycrystalline thin film photovoltaic cells [30], apart from amorphous silicon [11]. The present status and future prospects of these three thin film cells have been reviewed recently by Arya [31]. Table I.I taken from Hill [11] lists the materials and efficiencies of devices available in the 1990's with module costs estimated for different annual production rates.

Promise of cost reduction of silicon cells lies in applying new techniques. Silicon cells have now exceeded their theoretical maximum efficiency reaching 24.2%. This involved a number of innovations, mainly in the optical engineering of the cells and using graded silicon wafers. To reduce the wafer preparation cost, waste and time, three technologies are being developed; casting the silicon directly into ribbons or wafers; the formation of a thin crystalline film of silicon on a ceramic substrate; and the use of silicon droplets to produce microcells which are then attached to a flexible substrate in a "solar sand paper" form. Amorphous silicon cells, which suffer from fast degradation when exposed to light, have been improved dramatically by adopting a multi-junction approach. Junctions of p-i-n/p-i-n structure were fabricated without increasing device total thickness.

Table I.I .. Materials and efficiencies of devices available in the 1990s with module cost estimated for different annual production rates [11].

Cell Material		η_c	η_m	Module costs (£ W_p^{-1} 1989)		
				1 MW_p pa	10 MW_p pa	100 MW_p pa
Silicon	single crystal	24	16	3	1.5	1.0
	polycrystalline	18	12	3	1.2	0.8
	amorphous	14	4	2	1.0	0.4
Copper Indium diselenide		14	>10	2	1.0	0.4
Cadmium telluride		14	>10	2	1.0	0.4
Concentrator cells	silicon	27	15-19	4	1.5	0.8
	gallium arsenide	29	--	3	1.2	0.7
	multijunction	37	--	4	1.0	0.5

An efficiency of 14% was achieved with a three junction design [11].

Interest in $CuInSe_2$ as a photovoltaic material increased when a single crystalline $CdS/CuInSe_2$ solar cell with 12% efficiency was demonstrated in 1975 [32]. Siemens Solar in Germany is concentrating its efforts on modules that use copper indium diselenide where efficiencies of 14% for single cells and 11% for modules have been demonstrated. Using a p-type material of 1 eV direct bandgap, $CuInSe_2$ cells have a higher current but a lower voltage than silicon cells. A considerable development of these cells have been achieved by introducing 20% gallium on indium sites to enlarge the material band gap and hence generate a higher voltage. Cells of over 10% efficiency have been demonstrated at Stuttgart University, Germany [11]. The theoretical efficiency for $CuInSe_2$ is 23.5%. It is expected that cells with conversion efficiencies in the 17-18% range will be demonstrated in the near future [30].

Despite of the fact that the theoretical efficiency for CdTe is 27.5% [33] (assuming no losses), the best thin film CdTe solar cell to date has a conversion efficiency of 14.6% [34]. A CdTe polycrystalline solar cell is being developed by BP, UK. Cells of 14% efficiency and modules of about 10% efficiency have been demonstrated. These cells have the structure of n-CdS/p-CdTe. The BP technology is significant because the materials are deposited by an electroplating process which promises very low cost in mass production [11]. Further details about the semiconductors and cells based on them are contained in chapter three.

Although it is thought that mass-production will reduce the cost of solar cells significantly, much remains to be done to achieve better solar cells with higher efficiencies at lower cost [35]. Day by day findings prove that there is still more to achieve and more to be explored. For example sunlight has a wide spectral range, so that there are inherent losses in conversion by a single bandgap where the maximum achievable efficiency is about 28%. If the sunlight is absorbed by a cascade of materials of decreasing bandgaps in a multi-junction cell, then in principle over 2/3 of the solar energy could be converted to electricity, leading to a further boost in photovoltaic conversion efficiency. Ongoing research is being carried out on so called "Tandem" cells. The cell involves layers of material that respond to different portions of the solar spectrum. For space applications, Boeing, in the U.S.A. have devised a two layered gallium arsenide and gallium antimonide cell that converts 37% of the light into electricity [35]. Even higher efficiencies (40%) should be achievable using the very latest developments exploiting p-i-n quantum well structures [36].

1.4. Present Work

As demonstrated in section 1.3, cadmium telluride is one of the top three contenders for efficient low-cost terrestrial solar cell applications. In fact it has

entered the market production line, which, apparently, means that the manufacturers think that further enhancement of device feasibility is more likely to be evolve through engineering and technical challenge rather than fundamental science. However, there is still plenty of scope for research into many aspects of the material and the associated device, such as reducing the material resistivity and providing the device with good ohmic contacts. A better understanding of the physics and chemistry of the device should lead to further breakthroughs. The gap of 13% between the theoretical efficiency and that already achieved experimentally shows that more effort is needed on device improvement. Of course, although this device is only commercially favored in thin film form, a deeper understanding of the basic phenomena involved should be derived from a single crystal based device, which would eliminate some undesirable factors. The primary motivation behind the present study of single crystal cells was to investigate the potential of CdTe for solar cells both from the material and device fabrication point of view.

This thesis begins with a general discussion of world energy needs and the role of renewable energy sources, mainly photovoltaic power, in an environmentally sensitive scenario. After a short review of the historical background of photovoltaic cells, a general overview of future developments in the field is introduced and finally it is concluded that the material under investigation is a strong candidate for future applications. The second chapter gives a brief review of the theory utilised in all three fields involved in the studies; i.e. material resistivity control; contact optimisation; and device operation. Chapter 3 starts with the specification of a good solar cell material and the role of CdTe and CdS in solar cells. Finally, CdTe based solar cells mainly of the CdS/CdTe type are reviewed putting strong emphasis on single crystal based devices. The details of the experimental and characterisation techniques employed are provided in chapters four and five.

Chapters 6 to 9 contain the original experimental results. In chapter 6 two post growth doping methods are described, a mechanism of phosphorus diffusion is suggested and a method of obtaining low resistive p-CdTe single crystals is proposed. The results of measurements of the electrical and structural properties of the resultant material are also presented. The following two chapters (7 & 8) present the results of two types of metal/CdTe:P contacts. Chapter 7 is concerned with the In/CdTe rectifying contact, which was useful in the initial optimisation of the material and its ohmic contacts. Ohmic contacts form the main topic in chapter eight, where the problem of obtaining low resistance contacts to p-CdTe is addressed and the approach of creating a tunneling type contact proved successful. To fulfil this objective five materials (Sb, Cu, Au, P and graphite) were investigated, and several treatments of the selected material were utilised.

The properties of the optimised photovoltaic cells are described in chapter nine. Internal device parameters were obtained using; current-voltage (I-V), capacitance-voltage (C-V), spectral-response (SR), and electron beam induced current (EBIC) measurements, further, both device series (R_s) and shunt (R_{sh}) resistances were extracted using a combination of experimental and numerical analysis. The current transport mechanism in the CdS/CdTe:P heterojunction was also explored.

The thesis concludes with a summary of the main objectives achieved during the course of this work and some suggestions for further work in the field.

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Chapter II

Related Theory

2.1. Preface

When the periodicity of a crystal potential is interrupted by some kind of defect such as a native defect or an impurity atom, new energy levels are created in a localised region of the crystal near the disturbance. These levels usually lie within the forbidden gap of a semiconductor and hence have important effects on the crystal properties and accordingly their applications.

In the present study phosphorus was introduced into CdTe bulk crystals and the resultant material was used to fabricate solar cells and Schottky diodes. In this chapter, the background theory used in analysing the results obtained is reviewed. This review is divided into three areas; materials, solar cells, and metal-semiconductor contacts.

2.2. Materials

In the p-type conversion process, material properties are altered, and the changes introduced were monitored using the characterisation techniques to be described in chapter five. However, some of the theoretical aspects used in the material analysis are reviewed in this section.

2.2.1. Electrical Conductivity and Hall Effect

Measurements of both conductivity and Hall coefficient and hence the carrier concentration can provide a great deal of information about a semiconductor. If the measurements are made as a function of temperature, it is possible to determine the ionization energy of the carriers and to some extent to

ascertain the carrier scattering mechanisms.

2.2.1.1. Electrical Conductivity

The dark conductivity of a semiconductor is generally defined as:

$$\sigma = nq\mu_n + pq\mu_p \qquad (2.1)$$

where n and p are the densities of the free electrons and holes, and μ_n and μ_p are their mobilities respectively. q is the electronic charge. In II-VI semiconductors the conductivity is normally dominated by one type of carrier, usually electrons, except for ZnTe which is usually p-type and CdTe which is amphoteric. For electron conduction only equation 2.1 reduces to:

$$\sigma = nq\mu_n \qquad (2.2)$$

The temperature dependence of the electrical conductivity is controlled by variations in the carrier concentration and their mobility.

The number of electrons in the conduction band can be evaluated as:

$$n = 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} \exp\frac{-(E_c - E_f)}{kT} \qquad (2.3)$$

or

$$n = N_c \exp\frac{-(E_c - E_f)}{kT}$$

where N_c, the effective density of states in the conduction band, is

$$N_c = 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} \qquad (2.4)$$

and m_e^* is the effective mass of the electrons, h is Planck's constant and E_c, E_f are the conduction and Fermi levels. By substituting this equation into equation 2.2,

we have

$$\sigma = q\,\mu_n N_c \exp\frac{-(E_c - E_f)}{kT} \tag{2.5}$$

which by taking logs reduces to

$$\ln\sigma = \ln(N_c\, q\,\mu_n) - \frac{(E_c - E_f)}{kT} \tag{2.6}$$

Assuming that m_e^* is a constant (equation 2.4), the effective density of states in the conduction band is proportional to $T^{1.5}$. For acoustic mode lattice scattering, where the mobility is proportional to $T^{-1.5}$, a plot of $\log(\sigma)$ versus reciprocal temperature should then show a straight line with a slope of $-(E_c-E_f)/k$. When the mobility is controlled by impurity scattering ($\mu \alpha T^{+1.5}$), a plot of $\log(\sigma T^{-3})$versus reciprocal temperature would be expected to yield a straight line with a slope of $-(E_c-E_f)/k$. In both cases, the slope enables the donor activation energy (E_c-E_f) to be evaluated.

To make the electrical conductivity ($\sigma = 1/\rho$) measurements, the Van der Pauw method [1] was used. The technique is discussed in chapter 5.

2.2.1.2. Hall Effect

By applying a magnetic field in the z-direction, B_z, and simultaneously an electric field in x-direction, the Hall effect can be measured. The magnetic field causes carriers to be deflected horizontally in the y-direction until an electric fied E_y is set up which exactly balances the deflecting Lorentz force, and an equilibrium state is then reached. Consider, an n-type semiconductor, when the forces on an electron are equated at equilibrium, then

$$B_z\, q\, v = E_y\, q \tag{2.7}$$

where v is the electron drift velocity.

The current density, J_x is given by

$$J_x = n q v \tag{2.8}$$

and from equations 2.7 and 2.8,

$$E_y = \frac{B_z J_x}{n q} \tag{2.9}$$

The Hall coefficient R_H is defined as the ratio of the electric field to the magnetic field per unit current density, i.e.,

$$R_H = \frac{E_y}{B_z J_x} = \frac{V_y d}{B_z I_x} \tag{2.10}$$

where d is the sample thickness and V_y the voltage set up between probes in the y-direction is known as the Hall voltage. By comparing equations 2.9 and 2.10, we get

$$R_H = \frac{1}{n q} \tag{2.11}$$

Since all the parameters in equation 2.10 are measurable, R_H and hence the carrier concentration (n) can be obtained.

From equations 2.2 and 2.11,

$$R_H \sigma = \mu_H \tag{2.12}$$

which is called the Hall mobility.

For the four ohmic contacts A,B,C, and D in the van der Pauw technique, the resistivity and Hall coefficient may be measured as follows; If we define the resistance R_{ABCD} as the potential drop across AB per unit current through CD, the resistivity is given by [2]

$$\rho = \frac{\pi d (R_{ABCD} + R_{BCDA})}{2 \ln 2} f\left(\frac{R_{ABCD}}{R_{BCDA}}\right) \quad (2.13)$$

where f is the correction function defined by the equation

$$\frac{R_{ABCD} - R_{BCDA}}{R_{ABCD} + R_{BCDA}} = \frac{f}{\ln 2} \operatorname{arccosh}\left[\frac{\exp(\ln 2/f)}{2}\right] \quad (2.14)$$

The correction function, f has been shown to follow the approximation [3]:

$$f \approx 1 - \left[\frac{R_{ABCD} - R_{BCDA}}{R_{ABCD} + R_{BCDA}}\right]^2 ln2 - \left[\frac{R_{ABCD} - R_{BCDA}}{R_{ABCD} + R_{BCDA}}\right]^4 \left[\frac{(ln2)^2}{4} - \frac{(ln2)^3}{12}\right] \quad (2.15)$$

These calculations were performed with the assistance of a computer.

The Hall mobility is given by

$$\mu_H = \frac{d \Delta R_{DBAC}}{B \rho} \quad (2.16)$$

where the change in resistance R_{BDAC} on application of a magnetic field, B is ΔR_{BDAC}.

2.2.2. Carrier Mobility

When a semiconductor is subjected to an electric field E, the additional velocity that the carriers experience is called the drift velocity. If this velocity is small compared to the mean thermal velocity, then

$$v = \mu E \quad (2.17)$$

where v is the drift velocity and μ is a parameter called the drift mobility.

In solids, at high temperatures (>150K) lattice vibrations and lattice deformation play the dominant role in providing the damping force which

prevents unlimited acceleration of an electron and brings it to a steady value. Imperfections due to native defects or substitutional impurities can also dominate the carrier scattering and this normally happens at lower temperatures (i.e. <100K). In heavily doped material, charged impurity scattering may become important at room temperature. Scattering phenomena influence the mean free time, τ, between collisions. The mobility is related to the collision time by the equation

$$\mu = q\tau / m_e^*$$

Table II.I .. Summary of scattering mechanisms [2].

Scattering Mechanism	$\mu \alpha (m_e^*)^x T^y$	
	x	y
Polar	-3/2	expone-ntial
Piezoelectric	-3/2	-1/2
Acoustic	-5/2	-3/2
Ionised Impurity	-1/2	3/2
Neutral Impurity	1	indep-endent

There are several scattering mechanisms which can limit the carrier mobility. A short description follows and only the relevant results will be given here. As stated earlier, carrier mobility in solids is mainly limited by lattice or impurity scattering or perhaps a combination of both. A summary of scattering mechanisms is shown in table II.I.

(a) Lattice Scattering or electron-phonon Interaction

There are three important lattice scattering mechanisms namely optical, deformation potential and piezoelectric scattering.

i) Optical Phonon Scattering: Optical phonon scattering is also

known as polar optical mode scattering. It is associated with the vibration of two atoms in a unit cell in anti-phase which collectively produces an optical phonon. In compound semiconductors, adjacent atoms are oppositely charged and this allows an electrostatic potential to be associated with an optical phonon. The magnitude of this potential is dependent upon the degrees of ionicity of the bonding and this kind of scattering is therefore important in II-VI compounds. The effective charge on each ion, and hence the electron-lattice interaction, can be related to the difference between the static and optical dielectric constants. According to Howarth and Sondhemier [4], the strength of the interaction between an electron and the optical modes is characterised by a coupling constant α defined by the relation

$$\alpha = \left[\frac{q^2}{\hbar}\right]\left[\frac{m_e^*}{2\hbar w_1}\right]\left[\frac{\epsilon_{s'} - \epsilon_\infty}{\epsilon_{s'}\,\epsilon_\infty}\right] \qquad (2.18)$$

where $\epsilon_{s'}$ and ϵ_∞ are the static and the optical (high frequency) dielectric constants respectively, and $\hbar w_1$ is the energy of the optical mode (L.O) phonon. In non-polar crystals $\epsilon_{s'} - \epsilon_\infty$ is small, and α is therefore small, but in polar crystals it can assume a value of just less than unity. The expression for the mobility limited by optical mode scattering proposed by Howarth and Sondhemier [4] is

$$\mu_{OPT} = \left[\frac{1}{2\,\alpha\, w_1}\right]\left[\frac{q}{m_e^*}\right]\left[\frac{8}{3\sqrt{\pi}\sqrt{z}}\right]\psi(z)\,(e^z - 1) \qquad (2.19)$$

where z is the ratio of the Debye temperature to the lattice temperature (i.e. $\theta_D/T \ \ or \ \ hw_1/kT$), and $\Psi(z)$ is a factor, varying as a function of z from 0.6 to 1 over the temperature range involved [5].

ii) Piezoelectric Scattering: This mechanism is confined to crystals which lack inversion symmetry. These are usually ionic or partly ionic and so such scattering is also important in II-VI compounds. The interaction arises because acoustic modes generate regions of compression and rarefaction in a crystal. In piezoelectric crystals, this leads to electric fields. All the II-VI compounds are piezoelectric although those with the cubic structure are less so than the hexagonal ones. Harrison [6] gives the mobility limited by piezoelectric scattering as

$$\mu_{PIE} = \frac{0.044\ \rho\ C_L^2\ \hbar^2\ \epsilon_{s'}^2}{q\ C^2\ (m_e^{*3}\ k\ T)^{1/2}} \qquad (2.20)$$

where

ρ = density of the semiconductor

C_L = longitudinal acoustic wave velocity, and

C = piezoelectric electrochemical coupling constant.

iii) Acoustic Phonon Scattering: For semiconductors in which the bonding is primarily covalent, electrons are scattered predominantly by longitudinal acoustic (L.A) phonons. These L.A modes produce compressions and dilations which create local deformations in the dielectric constant as well as changes in the width of the bandgap.

The L.A phonons are the same as those involved in piezoelectric scattering. The deformation produces a variation in the kinetic energy of an electron as it passes through the crystal and the resultant interaction is known as acoustic phonon scattering. The main parameter involved in this type of scattering is the deformation potential E_1, which gives a measure of the change in position of the conduction band edge due to change in the volume of the unit cell. It is expressed as $-V(dE_c/dV)$. This subject was first introduced by Shockley and Bardeen [7] who proposed the following equation for the mobility limited by acoustic phonons

$$\mu_A = \left[\frac{8\pi}{m_e^{*5}(kT)^3}\right]^{\frac{1}{2}} \left[\frac{q\hbar^4 \rho C_L^2}{3E_1^2}\right] \qquad (2.21)$$

b) Impurity Scattering

i) Ionised Impurity Scattering: This type of scattering results from either deliberately introduced impurities or lattice defects generated by non-stoichiometry of the compounds. The defect can be positively or negatively charged and thus deflect the path of passing electrons. Conwell and Weisskop [8] derived an equation for the mobility limited by this kind of process by following the mathematical arguments used by Rutherford in his model for alpha-particle scattering. However, Brooks and Herring developed an alternative procedure [9] which takes account of the screening of the coulomb field of ionised impurities by free electrons. They produced the following equation

$$\mu_I = \left[\frac{2^7 (kT)^3}{\pi^3 m_e^*}\right]^{\frac{1}{2}} \quad \frac{\epsilon_{s'}^2}{q^3 N_i}\left\{\ln\left[\frac{6 m_e^* \epsilon_{s'} (kT)^2}{q^2 h^2 n' (2 - n'/N)}\right]\right\}^{-1} \tag{2.22}$$

for a compensated semiconductor, where $N_i = Z_A N_a + Z_B N_d$, N_a and N_d being the number of ionised acceptors and donors per unit volume, and Z_A and Z_B are the respective effective charges, n' = number of free carriers per unit volume (i.e. n+p) and $N = |N_d - N_a|$.

ii) Neutral Impurity Scattering: This type of scattering normally occurs at very low temperature. As the temperature of a semiconductor is lowered, carriers freeze out into impurity centres. The interaction of the electrons with neutral impurities is analogous to electron scattering by hydrogen atoms. Erginsoy [10] proposed the equation for this type of scattering as follows

$$\mu_N = \frac{m_e^*}{20 N \epsilon_{s'}} \left[\frac{q}{\hbar}\right]^3 \tag{2.23}$$

where N is the number of neutral impurity atoms per unit volume. However, Sclar [11] introduced a rather different approach, but this is only important at very low temperature. Once again the mobility is temperature independent.

2.3. Solar Cells

A solar cell makes use of the photovoltaic effect [1]; namely the absorption of light in a photosensitive material to create positive and negative charges (EH pairs) which can be separated by a built-in-field to develop a photovoltage and photocurrent, so allowing power to be delivered to an external load. In essence a solar cell is a diode that produces useful electricity from the absorption of solar radiation.

Although there are three types of junctions that may be used as photovoltaic cells, the following theoretical sections will be concerned with heterojunction cells. That is because the CdS/CdTe structure is of this type.

A heterojunction is simply a junction formed between two dissimilar semiconductors. The heterojunction is referred to as isotype if the two semiconductors have the same type of conductivity, other wise it is referred to as an anisotype. In 1951, Shockley proposed the abrupt heterojunction to be used as an efficient emitter-base junction in a bipolar transistor [12]. This was followed by Gubanov's theoretical work on heterojunctions [13]. Kroemer [14] later analysed a similar, although graded, heterojunction as a wide-gap emitter. Since then heterojunctions have been extensively studied for applications such as light-emitter diodes, photodetectors and solar cells. Heterojunctions have been reviewed by Milnes and Feucht [15], Sharma and Purohit [16] and Casey and Panish [17].

2.3.1. Solar Cell Structure

A typical configuration of a solar cell is given in figure 2.1. The absorber, sometimes known as the emitter absorbs the incident light, generating minority carriers, a proportion of which diffuses to the junction. The magnitude of the sign of the diffusion current is determined by the minority carrier density at the absorber-junction interface. The absorber is generally chosen to be a p-type

material because of the large diffusion lengths for minority electrons. The essential parameters of the absorber-generator are its energy gap (i.e. the threshold energy for the production of electron-hole pairs) and its absorption coefficient.

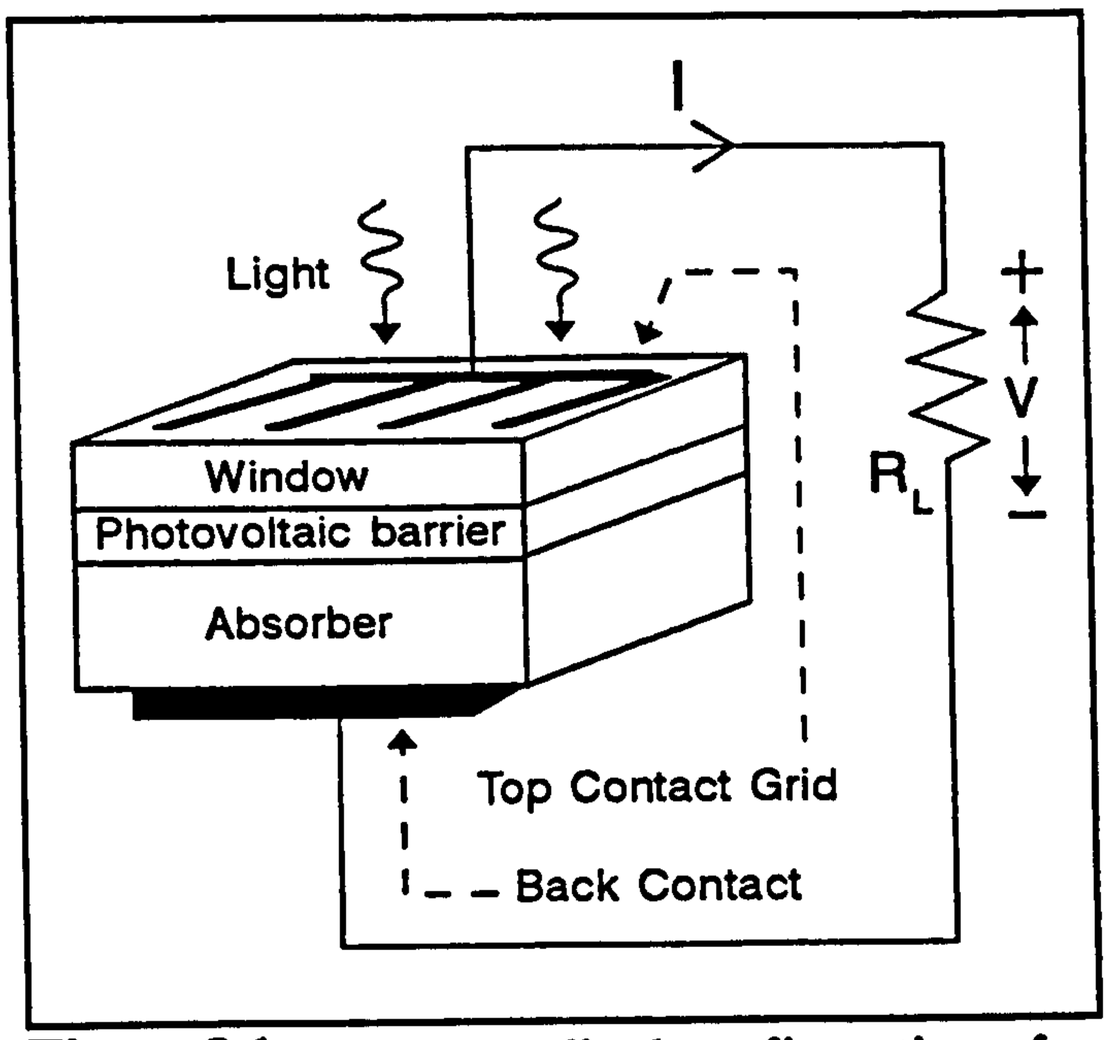

Figure 2.1 .. A generalised configuration of a solat cell.

The junction is the space charge region in which the minority carriers from the emitter are separated from the majority carriers and supplied to the collector for transmission to the external circuit. The junction provides almost all the voltage drop of the cell. The junction may be described as abrupt or graded, depending on whether the impurity concentration gradient across the junction changes from p to n abruptly or gradually. The three most common types of junction or barrier are; homojunctions, heterojunctions, and Schottky barriers.

The semiconductor layer on the other side of the junction interface from the absorber is called the collector-converter. The primary role of the collector is to collect the minority carriers and convert them into majority carriers. This requires that the collector be of opposite conductivity type so that the minority carriers swept across the junction become majority carriers, thus preventing their recombination before completing the external circuit.

The properties of the junction are strongly influenced by the properties of the semiconductors forming the junction, especially the electron affinities and the lattice parameters of the two materials (in hetero-junctions).

The fourth non-functional part of a solar cell which affects device

performance is provided by the metal electrodes to the absorber and collector. For an efficient performance good quality contacts (i.e. low resistance ohmic contacts) are necessary.

2.3.2. Dark Current Mechanisms

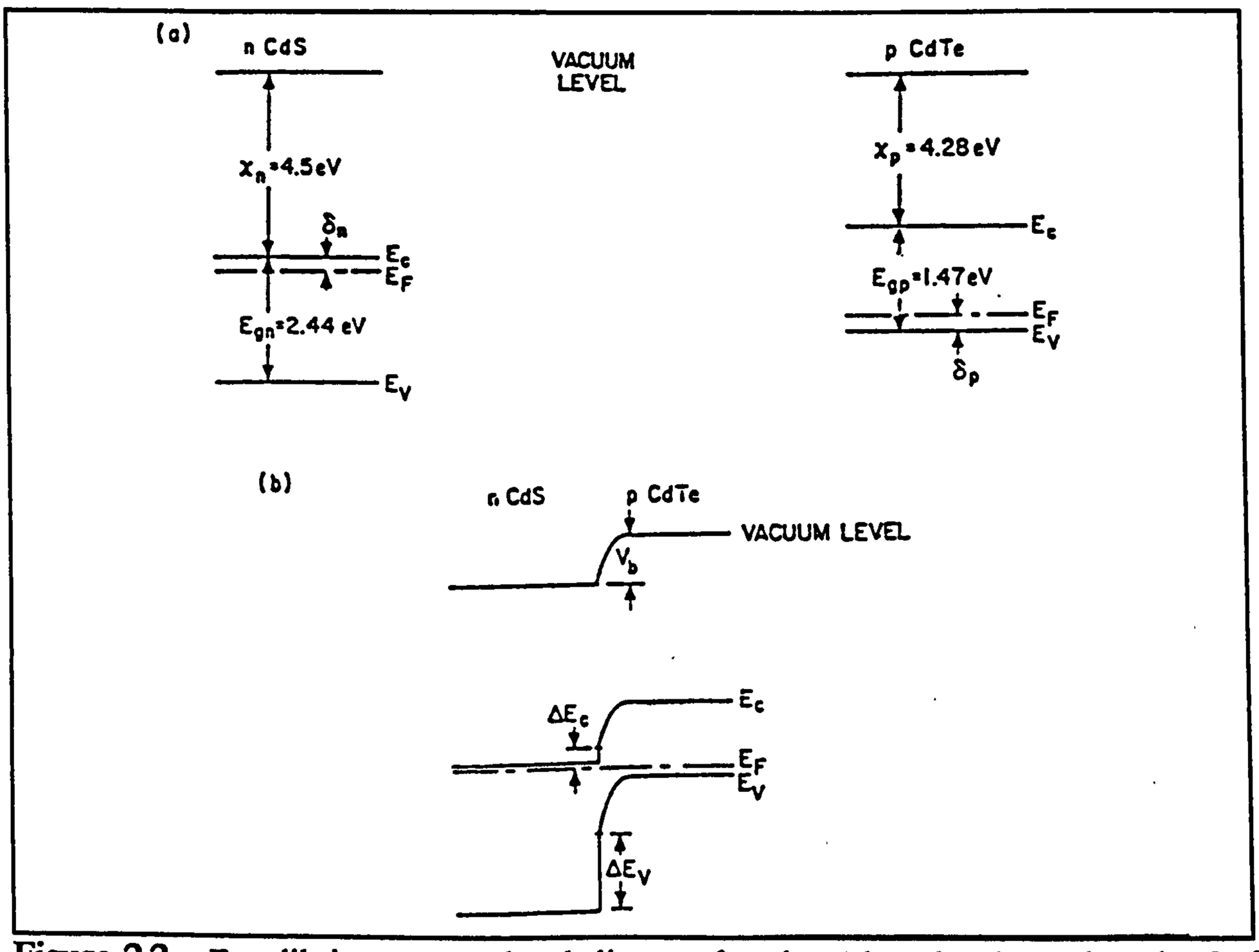

Figure 2.2 .. Equalibrium energy band diagram for the CdS/CdTe heterojunction [ref 21], where a) before and b) after the formation of an abrupt p-n junction.

The injection current model for a heterojunction was first developed by Anderson [18,19] as an extension of the conventional model for homojunctions [20], with barrier heights evaluated in terms of the energy band profile. When the effects of dipoles and interface states are negligible, the energy band profile of the n-CdS/p-CdTe heterojunction at thermal equilibrium and zero-bias is as shown in figure 2.2(a) and (b) before and after the formation of an abrupt junction [21]. Both the semiconductors are characterised by their electron

affinities, bandgaps and work functions. In this (ideal) situation the barrier height is given by; [21,22]

$$V_b = E_{gp} + \Delta E_c - \delta_n - \delta_p \tag{2.24}$$

where ΔE_c is the conduction band discontinuity at the hetero-interface, and δ_n and δ_p are the displacements of the Fermi level from the conduction and valence band edges in the n(CdS) and p(CdTe) type materials, respectively. E_{gp} is the bandgap of p-type material. The discontinuities are given by;

$$\Delta E_c = \chi_p - \chi_n \tag{2.25}$$

$$\Delta E_v = (E_{gn} - E_{gp}) - \Delta E_c \tag{2.26}$$

where E_{gn} is the band gap of the n-type material, and χ_p, χ_n are the electron affinities of the p and n-type materials, respectively.

2.3.2.1. Current-Voltage and Charge Transport Mechanisms

The current-voltage relationship in heterojunctions takes the form; [16,21]

$$J = J_{oo} \exp\left(\frac{-qV_{bp}}{kT}\right)\left[\exp\left(\frac{qV_p}{kT}\right) - \exp\left(\frac{-qV_n}{kT}\right)\right] \tag{2.27}$$

where

$$J_{oo} = XqD_nN_D/L_n \tag{2.28}$$

and

$$V_{bp} = K_p V_b \tag{2.29}$$

where $K_p = (1 + N_A \varepsilon_p / N_D \varepsilon_n)^{-1}$

$$V_p = K_p V \tag{2.30}$$

$$V_n = K_n V \tag{2.31}$$

and $K_n = 1 - K_p$

V_{bp} is the portion of the built-in voltage on the p-side of the junction; V_p and V_n are the portions of the applied voltage appearing on the p and n-sides of the junction; X is the transmission coefficient for electrons to pass the interface; D_n and L_n are the diffusion constant and diffusion length, respectively, for electrons in the p-type semiconductor. The contribution to the current from the injection of holes into the wider bandgap semiconductor is negligible because of the large energy barrier to hole injection arising from ΔE_v. When the n-type (CdS) is highly doped with respect to the p-type semiconductor, the expression for the current-voltage simplifies to:

$$J = J_o\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{2.32}$$

where

$$J_o = \left(\frac{XqN_D D_n}{L_n}\right)\exp\left(\frac{-qV_b}{kT}\right) \tag{2.33}$$

The energy band discontinuities and the appearance of interface states complicate the formulation of the recombination current. Recombination can take

place either through the interface states or in the space charge region, and is affected by the band profile within the junction region. Dolega [23] proposed a recombination current model which is based on the assumption that the thermal emission of carriers takes place into a thin region at the junction where the recombination velocity is high due to the interface states. This model simply describes the junction as two back-to-back Schottky diodes, having the boundary carrier concentrations dependent upon the applied bias. Similar treatments of the current transport assuming a metal-like thin layer of the recombination centres at the junction were developed by Oldham and Milnes [24] and Donnelly and Milnes [25]. Using Dolega's theory, Van Opdorp [26] derived an expression for the recombination current of the form [16,21]:

$$J = J_o\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{2.34}$$

where

$$J_o = J_{oo}\exp\left(\frac{-qV}{nkT}\right) \tag{2.35}$$

The diode factor n (which lies between 1 and 2) is a function of the imperfection densities in the two semiconductors and J_{oo} is a weak function of temperature. The recombination current within the depletion region can be approximated by the expression for the homojunctions, which in the dark under forward bias is given by the relation [21]:

$$J = \frac{qn_iW}{\sqrt{\tau_{p_o}\tau_{n_o}}}\left[\frac{2\sinh(qV/2kT)f(b)}{q(V_b - V)/kT}\right] \tag{2.36}$$

where W is the depletion region width, τ_{p_o} and τ_{n_o} are the minority carrier

lifetimes on the two sides of the junction, V is the voltage across the junction, V_b is the junction built-in voltage, and the factor f(b) is a function involving the trap level and the two lifetimes as follows:

$$f(b) = \int_0^\infty \frac{dx}{x^2 + 2bx + 1} \tag{2.37}$$

$$b = \exp(-qV/2kT)\cosh[(E_t - E_i)/kT + (\frac{1}{2})\ln(\tau_{p_o}/\tau_{n_o})] \tag{2.38}$$

where E_i is the intrinsic Fermi level.

The Sah et al (S-N-S) theory [49] was extended by Choo [27] to asymmetric junctions where the trap levels are not located at mid-gap, doping levels on each side of the junction are unequal, and the lifetimes τ_{p_o} and τ_{n_o} are also different. The derived dark current expression is essentially the same as equation 2.36, except the factor f(b) is smaller in magnitude than that obtained by Sah et al, i.e. the effect of junction asymmetries is to lower the recombination current below the value predicted by the S-N-S theory. The recombination current expressed by relation 2.36 can be simplified using the following assumptions:

(a) when $N_D >> N_A$ the depletion layer width W is given by:

$$W = \left(\frac{2\varepsilon}{qN_A}\right)^{\frac{1}{2}} (V_b - V)^{\frac{1}{2}} \tag{2.39}$$

(b) for an applied voltage $V >> 2kT/q$ (0.05 V at 300K).

$\sinh(qV/2kT)$ simplifies to $1/2\exp(qV/2kT)$. Under these conditions, the recombination current is given by:

$$J = J_o \exp\left(\frac{qV}{2kT}\right) \tag{2.40}$$

where

$$J_o = J_{oo} \exp\left(\frac{-E_g}{2kT}\right) \tag{2.41}$$

and

$$J_{oo} = (kT)\left(\frac{2N_c N_v \varepsilon}{qN_A \tau_{p_o} \tau_{n_o}}\right)^{\frac{1}{2}} (V_b - V)^{-\frac{1}{2}} f(b) \tag{2.42}$$

where ε is the dielectric constant.

Another transport mechanism is provided by tunneling caused by electrons or holes tunneling from the conduction or valence band into energy levels within the bandgap, followed by either tunneling the remainder of the way into the opposite band or by a tunneling-recombination mechanism. The tunneling mechanism to describe the current-voltage characteristics of an abrupt heterojunction was first reported by Rediker et al [28]. The tunneling current for a heterojunction is essentially the same as for a homojunction except that the number of states responsible for tunneling is much higher, due to interface states; and the tunneling energy barrier is modified by a distribution coefficient [21]. For $N_D >> N_A$, the tunneling current is represented by [15,22]:

$$J = J_o \exp(\alpha K_p V) \tag{2.43}$$

where

$$J_o = BXN_t \exp(-\alpha V_b) \tag{2.44}$$

$$\alpha = \left(\frac{4}{3h}\right)\left(\frac{m^* \varepsilon_p}{N_A}\right)^{\frac{1}{2}} \tag{2.45}$$

here ε_p and N_A are the dielectric constant and the doping densities respectively of the p-type semiconductor. The tunneling current may also be expressed as [21]:

$$J = J_{oo} \exp(\beta T) \exp(\alpha K_p V) \tag{2.46}$$

where

$$\beta = -\alpha \frac{\partial E_{gp}}{\partial T} + \frac{\partial \Delta E_v}{\partial T} - \frac{\partial \delta_n}{\partial T} - \frac{\partial \delta_P}{\partial T} \tag{2.47}$$

In addition to the tunneling of carriers, a multi-step tunneling recombination process has been proposed by Riben and Feucht [29,30]. The resultant current-voltage relation is similar to equation 2.46. If a number of tunneling steps are involved, the coefficient α is modified by the number of steps R so that α becomes [30,31]:

$$\alpha^* = \alpha / (R)^{\frac{1}{2}} \tag{2.48}$$

Adirovich et al [31] used the model expressed by equation 2.46 and 2.48 to explain the behaviour of CdS/CdTe heterojunctions.

2.3.2.2. Capacitance-Voltage Characteristics

The depletion width and capacitance of a p-n junction can be obtained by solving Poisson's equation for either side of the junction. An exact solution of the

equation (which requires numerical techniques) is generally not necessary, since approximate analytical solutions are adequate for most cases of interest. It is common to assume that in the space charge region, all the donors and acceptors are ionized and for space charge computations, the free carrier density can be neglected. Thus for a homojunction Poisson's equation can be written as [20,32]:

$$-\frac{\partial^2 V}{\partial x^2} = \frac{\rho}{\varepsilon \varepsilon_o} = \frac{q}{\varepsilon \varepsilon_o}[(p(x)-n(x))+N_D(x)-N_A(x)]$$
$$= \frac{q}{\varepsilon_n \varepsilon_o} N_D(x) \quad for\ 0<x<x_n \qquad (2.49)$$
$$= \frac{q}{\varepsilon_p \varepsilon_o} N_A(x) \quad for\ -x_p<x<0$$

In this case the origin has been taken as the junction plane, ρ is the charge density, ε_o is the permittivity of free space, x_n and x_p are the widths of the space charge region in the n and p materials respectively. The variation of $N_D(x)$ and $N_A(x)$ is generally assumed to be either a step function (abrupt junction) or a linear function of x (graded junction).

For heterojunctions the abrupt approximation is assumed to be valid, although some intermixing of the two materials on an atomic scale probably does occur. Assuming however, that the abrupt approximation applies, charge neutrality demands that

$$N_D\, x_n = N_A\, x_p \qquad (2.50)$$

using equations 2.49 and 2.50 the width of each space charge region, as a function of applied voltage can be written:

$$x_n = \left(\frac{2N_A \varepsilon_n \varepsilon_p (V_b - V)\, \varepsilon_o}{qN_D(\varepsilon_p N_A + \varepsilon_n N_D)} \right)^{\frac{1}{2}} \qquad (2.51)$$

$$x_p = \left(\frac{2N_D \varepsilon_n \varepsilon_p (V_b - V)\, \varepsilon_o}{qN_A(\varepsilon_n N_D + \varepsilon_p N_A)} \right)^{\frac{1}{2}} \tag{2.52}$$

The total width, W, of the depletion region therefore is given by:

$$W = x_n + x_p = \left(\frac{2\varepsilon_n \varepsilon_p (N_D^2 + N_A^2)(V_b - V)\, \varepsilon_o}{qN_D N_A(\varepsilon_n N_D + \varepsilon_p N_A)} \right)^{\frac{1}{2}} \tag{2.53}$$

The relative voltages supported on each side are given by:

$$\frac{V_{bn} - V_n}{V_{bp} - V_p} = \frac{N_A \varepsilon_p}{N_D \varepsilon_n} \tag{2.54}$$

where V_n and V_p are the voltage drops in the n and p materials respectively, and $V_b = V_{bn} + V_{bp}$.

For an abrupt heterojunction with uniform doping, the capacitance per unit area (where dipole and interface states effects are negligible), is given by [15,21]:

$$C = \left[\frac{qN_D N_A \varepsilon_n \varepsilon_p}{2(\varepsilon_n N_D + \varepsilon_p N_A)(V_b - V)} \right]^{\frac{1}{2}} \tag{2.55}$$

If $N_D >> N_A$ then the latter equation takes the form:

$$C = \left[\frac{q\varepsilon_p N_A}{2(V_b - V)} \right]^{\frac{1}{2}} \tag{2.56}$$

The net acceptor density N_A can thus be obtained from the slope of a plot of C^{-2} vs V, and the built-in voltage V_b from the intercept on the voltage axis. The result applies to a Schotty diode on a p-type semiconductor.

2.3.2.3. Electron Beam Induced Current

The basic idea behind this technique is presented mathematically below:

The continuity for minority carriers in a p-type semiconductor may be written as [20];

$$\frac{\delta \Delta n}{\delta t} = G - \frac{\Delta n}{\tau} + \Delta n \mu_n \nabla E + \mu_n E \nabla \Delta n + D_n \nabla^2 \Delta n \qquad (2.57)$$

where; Δn: excess electron population, G: electron-hole generation rate, τ: lifetime, μ_n: electron mobility, E: electric field, and D_n: Diffusion constant.

Assuming that the electric field E outside the depletion region is zero, the equation reduces in one dimension to:

$$\frac{\delta^2 \Delta n}{\delta x^2} - \frac{\Delta n}{\tau D_n} = -\frac{G}{D_n} \qquad (2.58)$$

This can be solved with the following boundary conditions;

$\Delta n\ (x = \infty) = 0$

$\Delta n\ (x = 0) = \Delta n_o$

to give

$$\Delta n(x) = G\tau + (\Delta n_o - G\tau) \exp\left(\frac{-x}{L_n}\right) \qquad (2.59)$$

A similar relation can be established for n-type material. Since the current density J is related to Δn by;

$$J_n = q D_n \nabla \Delta n(x)\,|_{x=0} \qquad (2.60)$$

then

$$J_n = J_{(o)} \exp\left(\frac{-x}{L_n}\right) \quad (2.61)$$

where

$$J_{(o)} = \frac{e D_n (\Delta n_o - G\tau)}{L_n} \quad (2.62)$$

Equation 2.61 forms the basis of the present measurements. In practice the device was fractured perpendicular to the junction plane. A line scan was carried out across the junction surface and from this current measurements were made as a function of distance. A plot of $Ln\ J_x / J_o$ versus x was then constructed in which the gradient gave a measurement of $1/L_n$.

2.3.4. Light Current Mechanism

2.3.4.1. Equivalent Circuit

When a diode is exposed to light of sufficient energy ($h\nu > E_g$) electron-hole pairs are generated. These carriers diffuse to the junction where they are separated to produce useful electrical energy. This can be modelled as a light dependent current generator connected in parallel with the diode. This is illustrated in the solar cell equivalent circuit shown in figure 2.3 which includes series and shunt resistance components.

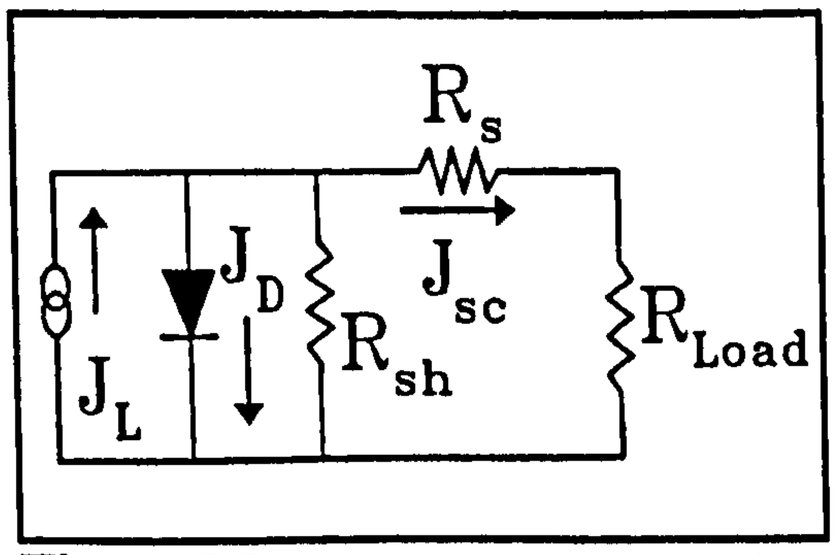

Figure 2.3 .. An equivalent circuitof a solar cell.

The general expression for the total current through the illuminated diode

is given by the following equation which is a linear superposition of the dark and light generated currents [33]

$$J - \frac{(V - JR_s)}{R_{sh}} = \sum_i J_{oi}\left[\exp\left\{\frac{q}{A_i kT}(V - JR_s)\right\} - 1\right] - J_L(V) \qquad (2.63)$$

where J_L is the light generated current. This is discussed in the following section, with reference to window-absorber heterojunction solar cells. Under illumination, the dark current voltage characteristics are translated by the amount of light current. The dark and light current-voltage characteristics for an ideal case are given in figure 2.4.

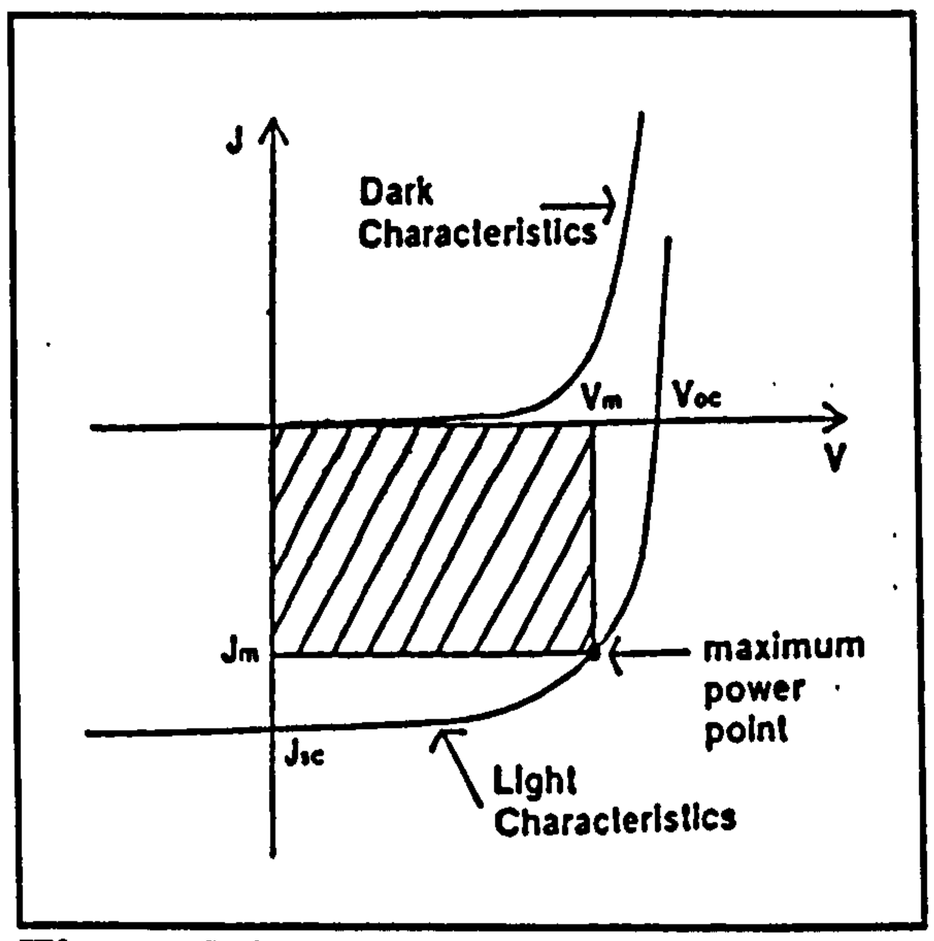

Figure 2.4 .. Typical dark and light characteristics of an ideal solar cell.

2.3.4.2. Solar Cell Parameters

The performance parameters of a solar cell are derived from the output characteristic. Usually four main parameters are used as figures of merit.

(1) Short circuit current (I_{sc}):

This is the photocurrent output of a solar cell when the load impedance is much smaller than the device impedance, or it may be defined as the photocurrent flowing through the junction at zero applied bias. In ideal conditions (i.e. when the series and shunt resistance effects are negligible) it is equal to the light generated current I_L and is proportional to the incident photon flux with energy greater than or equal to the energy gap of the absorber.

In essence, the short circuit current is determined by the spectrum of the light source and the spectral response of the device.

The spectral response in turn depends on the optical absorption coefficient α, the junction depth , the width of the depletion region, the lifetimes and mobilities on both sides of the junction, the presence or absence of electric fields in both the semiconductors on either side of the junction, and the surface recombination velocity [34].

(2) Open Circuit Voltage (V_{oc}):

The open circuit voltage is the output voltage of the device under illumination when the load impedance is much greater than the device impedance, i.e. it is the voltage across the terminals of an illuminated solar cell at zero current flowing through the junction. The open circuit voltage of a p-n junction solar cell is directly related to the bandgap of the semiconductor through the barrier height at the junction and is often expressed in terms of the short circuit current I_{sc}, the reverse saturation current I_o and the ideality factor A as [35]:

$$V_{oc} = \frac{AkT}{q} \ln\left(\frac{I_{sc}}{I_o} + 1\right) \qquad (2.64)$$

It might appear from this equation that high values of A are desirable in obtaining high V_{oc} but this is not so. With large values of A, I_o increases and consequently the open circuit voltage is reduced. In contrast in an ideal junction, A is equal to unity and V_{oc} attains its highest value. The dark current I_o is mainly determined by the energy gap of the material and temperature; I_o decreases and V_{oc} increases with increasing energy gap or decreasing temperature. There is thus a trade-off between high V_{oc} with a large bandgap absorber and the high I_{sc} obtained from

narrow band materials.

(3) Fill Factor (FF):

Mathematically the fill factor is the ratio of the maximum electrical power output to the product of V_{oc} and I_{sc}. It describes the rectangularity or squareness of the photovoltaic output characteristic. The fill factor is mainly determined by the value of A, the series resistance R_s, and the shunt resistance R_{sh}. A high shunt resistance and low values of A and R_s are required for a high fill factor. High values of fill factor correspond to high rectangularity of the output characteristics, while small values result in softening of the characteristics.

(4) Efficiency (η):

This parameter describes the overall performance of a solar cell. The three parameters; I_{sc}, V_{oc}, and FF, determine the efficiency of a cell, which can be expressed as [36]:

$$\eta = \frac{I_{sc} \times V_{oc}}{P_{inc} \times Area} \times FF \qquad (2.65)$$

where P_{inc} is the incident radiation power density, usually expressed in mW/cm^2.

2.3.4.3. Generation and collection of photocarriers

Although the absorption of light takes place in both the absorber and the collector of a heterojunction solar cell, the analysis of photocarrier generation and collection is greatly simplified by assuming that the light is absorbed mainly in the absorber. In particular, for the CdS/CdTe cell the following assumptions are made [21]:

(i) light absorbed in the CdS (window layer) does not contribute to

the photocurrent; (ii) the CdTe layer is wider compared to the absorption length so that back surface effects can be neglected; (iii) there are no electric fields outside the depletion region; and (iv) the electric field is sufficiently strong in the depletion region to separate all carriers generated within it, or arriving at its boundaries [37].

The collection of photogenerated minority carriers in the CdTe (absorber) is evaluated by considering the contribution from two regions: (a) the depletion region, where the high junction field assists the carrier collection; and (b) the bulk, characterised by a constant minority carrier diffusion length. The collection of photogenerated carriers may thus be described as the product of two terms: a generation term representing the number of carriers generated by absorption of light; and a carrier collection term describing the fraction of carriers arriving at a specific boundary (i.e. crossing the junction).

If $\phi(\lambda)$ is the photon flux density incident on the CdTe and $\alpha(\lambda)$ is the optical absorption coefficient then the absorption of light in CdTe is described by the relation [21]

$$\phi(x) = \phi_o(\lambda) \exp[-\alpha(\lambda)x] \tag{2.66}$$

where $\phi(x)$ is the photon flux density at a distance x from the surface, $\phi_o(\lambda)$ is the photon flux entering the CdTe. The number of photons absorbed in the depletion region (width W) is $\phi_o[1-\exp(-\alpha W)]$ and the total generation of carriers in this region is therefore:

$$G_W = a_o \phi_o [1 - \exp(-\alpha W)] \tag{2.67}$$

where a_o is the quantum efficiency for the absorbed light to produce electron-hole pairs (the ratio of the number of charge carriers generated to the number of photons absorbed), and G_W is the number of carriers generated in the depletion

region. Since the bulk of the absorber semiconductor is assumed to be thick enough to absorb all the photons reaching it, then the total number of photocarriers generated in the bulk, G_B is:

$$G_B = a_o \phi_o \exp(-\alpha W) \tag{2.68}$$

Assuming total carrier collection, the photocurrent reaching the junction interface from the depletion region is directly proportional to the number of photons absorbed and is given by:

$$J_W = qG_W = qa_o \phi_o [1 - \exp(-\alpha W)] \tag{2.69}$$

The photocurrent due to the diffusion of photogenerated carriers (for the bulk) to the edge of the depletion region is [21,25]:

$$J_B = qG_B \left(1 + \frac{1}{\alpha L}\right)^{-1} \tag{2.70}$$

$$J_B = qa_o \phi_o \left(1 + \frac{1}{\alpha L}\right)^{-1} \exp(-\alpha W) \tag{2.71}$$

where L is the minority carrier diffusion length in the bulk CdTe. The total photocurrent to the junction interface, J_I, is therefore the sum of J_W and J_B, i.e.

$$J_I = qa_o \phi_o [1 - (1 + \alpha L)^{-1} \exp(-\alpha W)] \tag{2.72}$$

The recombination current J_R due to interface states can be expressed as:

$$J_R = qSn_I \tag{2.73}$$

where S is the recombination velocity and n_I is the density of minority carriers at the interface. Conservation of currents at the interface leads to the relation: where J_L is the current which enters the collector (CdS). The light current J_L may

$$J_I = J_R + J_L \tag{2.74}$$

be expressed as [21]:

$$J_L = q\, n_I \mu_e E_I \tag{2.75}$$

where μ_e is the electron mobility in the junction region and E_I is the electric field at the junction interface. Using equations 2.73-2.75, J_L can be written:

$$J_L = \left(1 + \frac{S}{\mu_e E_I}\right)^{-1} J_I \tag{2.76}$$

and substituting for J_I from equation 2.72, the photogenerated current reaching the CdS is:

$$J_L = q a_o \phi_o \left(1 + \frac{S}{\mu_e E_I}\right)^{-1} [1 - (1 + \alpha L)^{-1} \exp(-\alpha W)] \tag{2.77}$$

Equation 2.77 may be written as:

$$J_L = q a_o \phi_o h(V)\, g(V) \tag{2.78}$$

where

$$h(V) = \left(1 + \frac{S}{\mu_e E_I}\right)^{-1} \tag{2.79}$$

and

$$g(V) = [1 - (1 + \alpha L)^{-1} \exp(-\alpha W)] \tag{2.80}$$

The term g(V) represents the fraction of photogenerated minority carriers reaching the junction, and h(V) is the fraction of minority carriers that safely pass through the junction upon reaching it. The product of h(V) and g(V) is called the

collection function H(V) i.e.

$$H(V) = h(V)\, g(V) \tag{2.81}$$

2.3.4.4. Spectral Response and Quantum Efficiency

As described earlier, a solar cell is characterised by "external" or performance parameters such as its short circuit current, open circuit voltage etc. In addition, some "internal" quantities also exist of which the principal ones are the spectral response and the quantum efficiency.

The spectral response is the photocurrent collected at each wavelength relative to the number of photons incident of the surface of the device. The quantum efficiency (also known as the internal spectral response) is the ratio of the number of collected carriers to the number of photons which enter the cell [38]. Both the spectral response (in mA mW^{-1})and quantum efficiency express the solar cell's ability to convert light into electrical current and are a function of the wavelength of the incident light. The quantum efficiency gives a more physical insight into the actual behaviour of the cell while spectral response expresses conversion performance in units that can be measured, and which are of more interest to the user.

By definition, the quantum efficiency (spectral response corrected for reflection loss is:

$$Q(\lambda) = \frac{J_L}{q\,\Phi_o} \tag{2.82}$$

where ϕ_o is the photon flux entering the cell. The relation between incident photon flux ϕ_s and the photon flux entering the cell ϕ_o is given by:

$$\phi_o = \phi_s\,(1-R) \tag{2.83}$$

where R is the overall reflection loss. So substituting for J_L from equation 2.78 the

quantum efficiency can be expressed as:

$$Q(\lambda) = a_o H(V) \tag{2.84}$$

where a_o is the quantum efficiency of the absorbed light to produce electron-hole pairs, and is equal to unity. Thus $Q(\lambda)$ for the CdS/CdTe solar cell becomes:

$$Q(\lambda) = \left(1 + \frac{S}{\mu_e E_I}\right)^{-1} [1 - (1 + \alpha L)^{-1} \exp(-\alpha W)] \tag{2.85}$$

For CdS/CdTe heterojunction cells, the short wavelength cut-off of the spectral response is defined by the sharp absorption edge of the window material (CdS) and the shape of the long wavelength edge by the collection of charge carriers from the CdTe, given by the collection function H(V). The quantum efficiency is voltage dependent through the variation of the electric field at the junction and the width of the depletion region with applied bias.

2.4. Metal-Semiconductor Contacts

Contact technology is a most important area in relation to electronic materials, since practically all electronic devices require good electrical contacts. In some cases, it is essential to form contacts that give rise to an electrical barrier, a Schottky barrier, at the interface which allows current to flow in only one direction. The fundamental aspects of these will be considered briefly in section 2.4.1. In other applications, and this applies to solar cells, it is necessary for the contact to have a low resistance and to show "ohmic" behaviour. In solar cell work, the aim is usually to reduce the series resistance of the cell. Ohmic contacts will be discussed briefly in section 2.4.2.

2.4.1 Schottky Barriers

Because of their simple structure and relative ease of fabrication Schottky devices were used in the present study as a mean of characterising the materials. The first useful models to account for metal-semiconductor barriers were put forward by Mott (1938) and Schottky (1942). Schottky suggested that there would be a barrier (later called a Schottky barrier) at the contact due to stable space charges in the semiconductor [39]. In the Schottky model the density of charged impurities in the barrier region is assumed to be constant, so that the electric field increases linearly and the potential quadratically as the metal is approached. The basic theory and the theoretical development of rectifying MS contacts have been fully reviewed by Henisch [40].

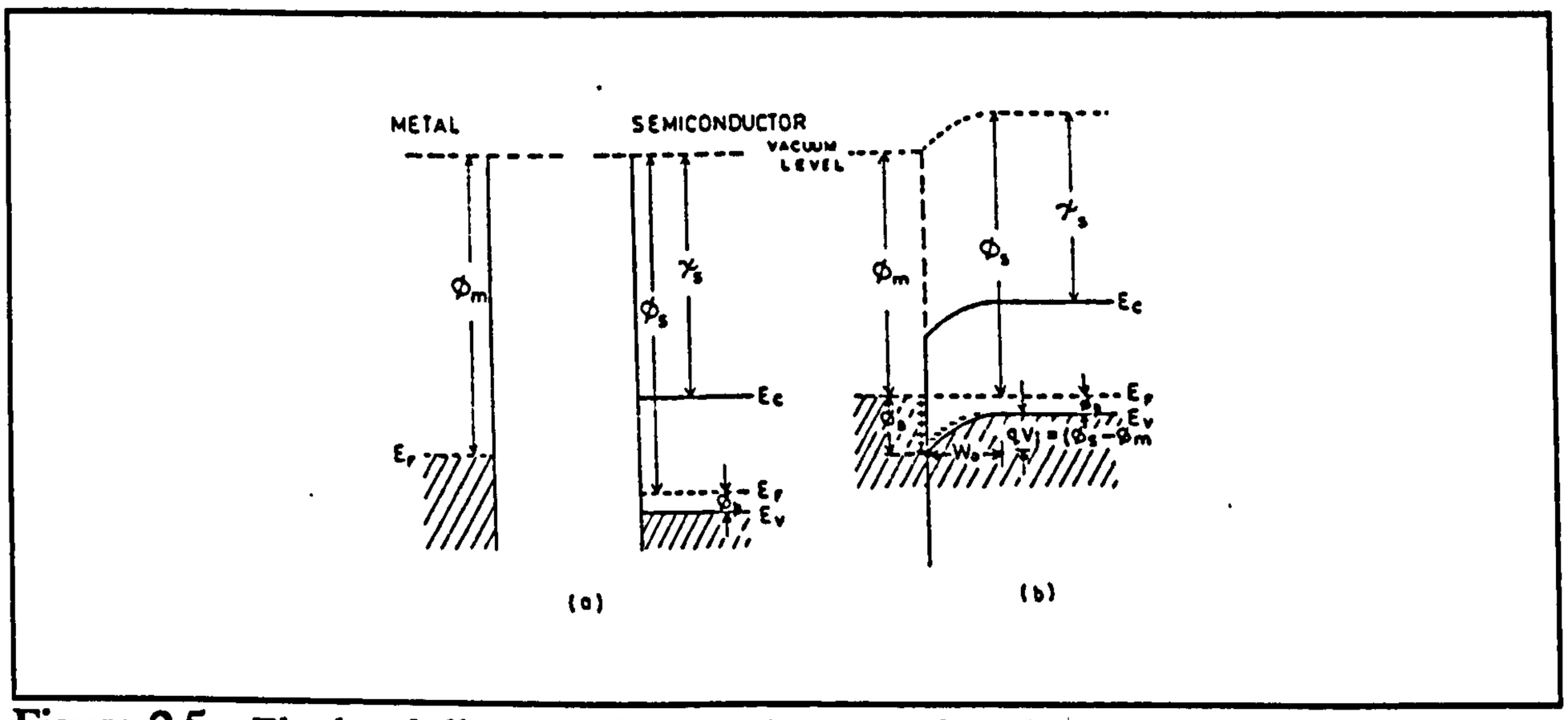

Figure 2.5 .. The band diagram of a metal and semiconductor before and after contact.

When an intimate contact is made between a semiconductor of work function ϕ_s and a metal of work function ϕ_m, a readjustment of charges takes place to establish thermal equilibrium. For a metal contact to a p-type semiconductor it is said that the contact will behave as a rectifier if $\phi_m < \phi_s$. The band diagram of a metal and semiconductor before and after contact is shown in figure 2.5. For an ideal contact between a metal and a p-type semiconductor, the

barrier height is expressed as

$$q\phi_{bp} = E_g - q(\phi_m - \chi) \tag{2.86}$$

In practice there will be surface states and if the density of surface states is sufficiently large, then the resulting surface charge will dominate the junction behaviour. As a result, the barrier height is determined by the semiconductor surface and will be independent of the metal work functions. The barrier height will also be reduced as a result of the image force, the so called Schottky effect.

2.4.1.1. Depletion Width and Capacitance

For an n-type semiconductor, the width W of the depletion region is given by Sze [20] as:

$$W = \sqrt{\frac{2\varepsilon_s}{qN_D}\left(V_{bi} - V - \frac{kT}{q}\right)} \tag{2.87}$$

where kT/q arises from the contribution of the majority carrier distribution tail. Thus the depletion width increases with reverse bias and is inversely proportional to N_D, the density of uncompensated donors. The change in W will lead to a corresponding change in capacitance. Neglecting the contribution of free carriers to the electrical field, and assuming that the surface density is low, ($<10^{12}$ cm^{-2} eV^{-1}) [41] and that all the donor impurities are ionised, then the capacitance of the barrier is only due to the space charge Q_{sc} (per unit area) and can be written as:

$$Q_{sc} = qN_D W = \left[(2q\varepsilon N_D\left(V_{bi} - V - \frac{kT}{q}\right)\right]^{\frac{1}{2}} \quad Col/cm^2 \tag{2.88}$$

and the depletion layer capacitance C per unit area is then

$$C = |\partial Q_{sc}| / \partial V = \left[\frac{q \epsilon_s N_D}{2(V_{bi} - V - \frac{kT}{q})} \right]^{\frac{1}{2}} = \frac{\epsilon_s}{W} \quad F cm^{-2} \qquad (2.89)$$

The depletion layer capacitance is inversely proportional to the depletion width W which in turn depends on the applied bias. The equation 2.89 is often written as

$$\frac{1}{C^2} = \frac{2(V_{bi} - V - \frac{kT}{q})}{q \epsilon_s N_D} \qquad (2.90)$$

providing that N_D remains constant throughout the depletion region. A plot of C^{-2} vs V is a straight line, the slope of which is

$$\frac{d(C^{-2})}{dV} = -\frac{2}{q \epsilon_s N_D} \qquad (2.91)$$

from which N_D can be calculated. Further parameters can be calculated from the plot, such as the width of the depletion region at zero bias from the intercept on the y-axis and the contact potential from the intercept on the voltage axis.

2.4.2. Ohmic Contacts

For a contact to be ohmic, the voltage drop across it must be much smaller than that across the device. It is also desirable that it should pass current equally in either direction, in other words, have a linear I-V characteristic. For solar cells, there is also the need that the contact should have a negligible photovoltaic effect. Following the Mott-Schottky theory, an ideal ohmic contact on a p-type material can be formed when $\phi_m > Eg + \chi_s$, see figure 2.6. In this case, a reservoir of carriers exists in the semiconductor near the interface, yielding an ohmic contact.

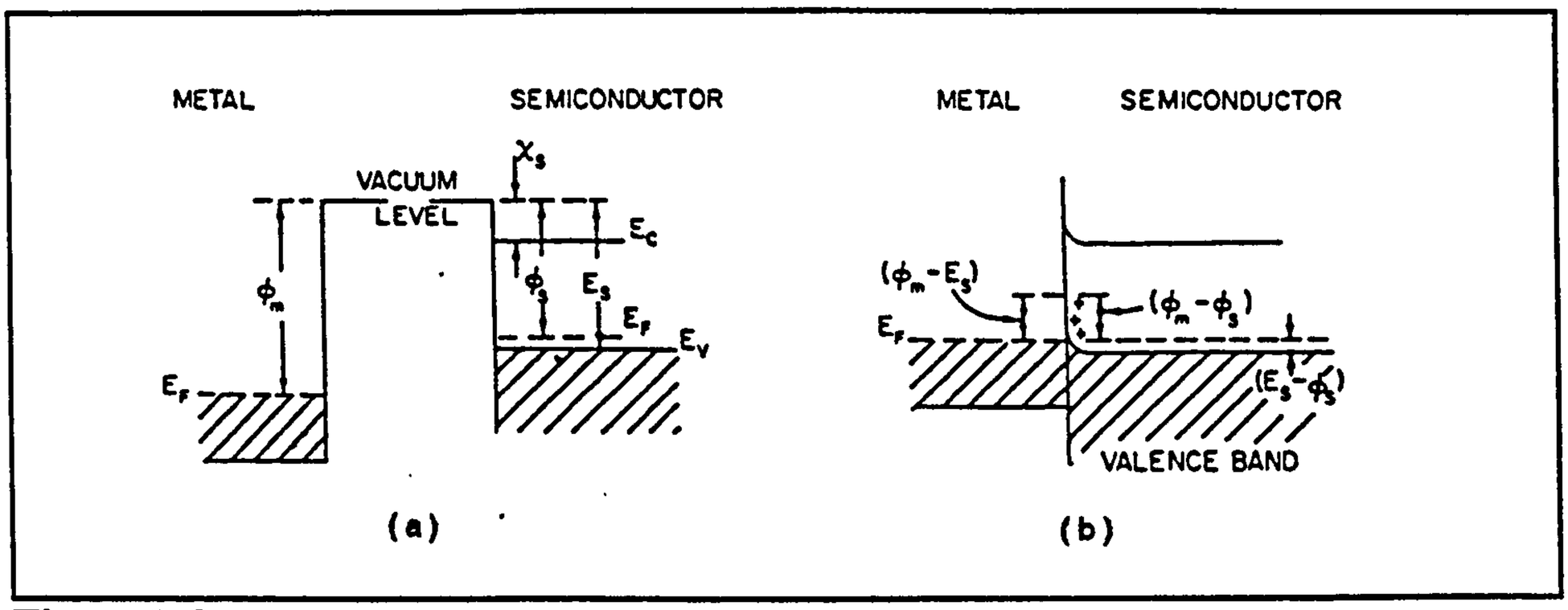

Figure 2.6 .. The band diagram of a ohmic contact formed between a metal and a p-type semiconductor; a) before and b) after contact.

Due to Fermi level pinning, the production of an ideal ohmic contact is rarely achieved.

In the present study the series resistance of a device was used as a measure for evaluating contact suitability. No special attention was given to the measurement of contact specific resistance, nevertheless, for identical devices with different ohmic contacting methods, changes in overall series resistance could be correlated with the contacting method in order to optimise p-CdTe ohmic contacts. This approach was applied in both solar cell and Schottky diodes.

A brief introduction to device resistance is given in the next sub-section, this is followed by short reviews of the theory behind the methods used in device series resistance evaluation.

2.4.2.1. Device Resistances

In real systems there are additional effects which may be lumped together in the form of a series resistance R_s and a shunt resistance R_{sh}, so that experimental behaviour may be approximated by the relation [42]:

$$J - \frac{(V - R_s J)}{R_{sh}} = \sum_i J_{oi} [\exp\{\alpha_i (V - J R_s)\} - 1] \qquad (2.92)$$

where the sum over i indicates various contributions to the diode current which can occur and α_i is written for $q/A_i kT$.

The series resistance of the diode arises from two major sources: (1) the resistance of the series components; and (2) of the electrodes and contacts to the external circuit. Shunt resistance arises from the current leakage paths within the diode. Generally, the shunt resistance in "good" diodes is so large that its effects are negligible. In cases where its effects are significant, gross defects in the junction are usually the case. The outer boundaries of a junction device inevitably permit some leakage of current, but even in single crystal diodes, some areas are found to have much higher leakage currents than average [43]. Surface damage during fabrication seems to play a significant role in reducing the shunt resistance in these areas [43,44].

2.4.2.1.1. Series Resistance of Solar Cells

In heat treated junctions, the shunt resistance is normally very high and its contribution towards the loss in fill factor is small compared with that of the series resistance. The role of the series resistance is to contribute to a loss in the output power P_o which is given by the expression, $P_o = IV$ where I and V are respectively the current and voltage at the maximum power point. The allowable power loss P_L due to a total series resistance r_s is, $P_L = I^2 r_s A$, where A is the solar cell area.

Wolf and Rauschenbach [45] developed a self consistent procedure to measure the series resistance of solar cells. With this method the photovoltaic output characteristic has to be measured at two different light intensities, the magnitude of which do not have to be known.

The basic equation describing the current-voltage characteristic of a solar cell neglecting series resistance and shunt resistance is:

$$I = I_o \left(e^{BV} - 1\right) - I_L \tag{2.93}$$

where $B = \frac{q}{AkT}$, and all other symbols stand for their normal quantities. Since the light generated current I_L is proportional to the intensity of the incident radiation up to extremely high light intensities [45], a change in the photovoltaic output characteristic under light intensity L_1 with a generated current I_{L1} to a light intensity L_2 generating a current I_{L2}, the current-voltage relation (equation 2.93) can be rewritten to be

$$I_1 = I_o \left(e^{BV_1} - 1\right) - I_{L1} \tag{2.94}$$

$$I_2 = I_o \left(e^{BV_2} - 1\right) - I_{L2} \tag{2.95}$$

Since V is the independent variable , one can choose:

$$V_1 = V_2 \tag{2.96}$$

and can set:

$$I_{L2} = I_{L1} + \Delta I_L \tag{2.97}$$

where ΔI_L is proportional to the difference in light intensity between levels 1 and 2. Subtracting equation 2.94 from equation 2.95 after introducing equation 2.96 and 2.97, one can obtain:

$$I_2 = I_1 - \Delta I_L \tag{2.98}$$

for all choices of $V_2 = V_1$. Equation 2.98 describes a translation of coordinate

system parallel to the current axis by the amount ΔI_L on the current axis.

For higher light levels, the effect of series resistance on the IV characteristic has to be included, due to the increased magnitude of the current I. Here

$$V' = V - IR_s \tag{2.99}$$

is the voltage across the p-n junction, which is larger than the terminal voltage V by the voltage drop in the series resistance. (Note the current I is a negative quantity, resulting in $V' \geq V$ for power generation in the solar cell.) The IV characteristic including the series resistance effect is

$$\begin{aligned} I &= I_o(e^{B(V-IR_s)} - 1) - I_L \\ &= I_o(e^{BV'} - 1) - I_L \end{aligned} \tag{2.100}$$

Introducing again two light levels 1 and 2, one obtains:

$$I_1 = I_o(e^{BV_1'} - 1) - I_{L1} \tag{2.101}$$

$$I_2 = I_o(e^{BV_2'} - 1) - I_{L1} - \Delta I_L \tag{2.102}$$

Again one chooses

$$V_2' = V_1' \tag{2.103}$$

and obtains the same translation as before $I_2 = I_1 - \Delta I_L$. Equation 2.99 results, however, in two different terminal voltages V_1 and V_2 for the two currents I_2 and I_1. From equations 2.103, 2.99 and 2.98, it follows that:

$$V_1 - I_1 R_s = V_2 - I_1 R_s + \Delta I_L R_s \tag{2.104}$$

which describes a constant relation ship between V_1 and V_2 for any choice of V_1. The constant of this relationship is proportional to the series resistance R_s and to the change in light level. Equation 2.104 thus describes a second translation of the coordinate system, this one parallel to the voltage axis by the amount:

$$V_2 = V_1 - \Delta I_L R_s \tag{2.105}$$

from which an estimate of R_s can be obtained.

2.4.2.1.2. Series Resistance in Schottky Diodes

Using V_D as the voltage applied across a Schottky diode, k the Boltzmann constant, and T the absolute temperature, the I-V relationship is expressed as

$$I = I_s \left[\exp \frac{qV_D}{nkT} - 1 \right] \tag{2.106}$$

and I_s is given by

$$I_s = A_{eff} A^{**} T^2 \exp\left(\frac{-q\phi_B}{kT} \right) \tag{2.107}$$

where A_{eff} is the effective area of the diode, A^{**} is the Richardson constant, and ϕ_B is the Schottky barrier height.

The effect of the diode series resistance R is usually modeled with a series combination of a diode and a resistor with resistance R through which a current I flows. The voltage V_D across the diode can then be expressed in terms of the total voltage drop V across the series combination of the diode and the resistor. Thus V_D=V-IR, and for V_D>3kT/q, the diode I-V relationship becomes:

$$I = I_s \exp\left[\frac{q(V-IR)}{nkT} \right] \tag{2.108}$$

Several methods have been proposed to extract the series resistance of metal-semiconductor devices [46-48]. The first was proposed by Norde [46]. His method was to extract R for ideal Schottky diodes (i.e. n=1). For diodes with n>1 cases, Sato and Yasumura [47] modified Norde's approach to extract the values of n, ϕ, and R from two experimental I-V measurements conducted at two different temperatures. Alternatively, S.K.Cheung and N.W.Cheung [48], proposed a method to determine the same factors from a single I-V measurement. The latter method was used in the present study to determine device series resistances, the basis of the method is introduced in the following paragraph.

Equation 2.108 can be rewritten in terms of current density ($J = I/A_{eff}$). Thus,

$$V = RA_{eff}J + n\phi_B + \left(\frac{n}{\beta}\right)\ln\left(\frac{J}{A^{**}T^2}\right) \qquad (2.109)$$

where

$$\beta = \frac{q}{kT} \qquad (2.110)$$

Determining equation 2.109 with respect to J and rearranging terms, we obtain

$$\frac{d(V)}{d(\ln J)} = RA_{eff}J + \frac{n}{\beta} \qquad (2.111)$$

Thus, a plot of $\frac{d(V)}{d(\ln J)}$ vs J will give RA_{eff} as the slope and $\overline{\beta}$ as the y-axis intercept.

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Chapter III

CdTe and CdS for Solar Cells

3.1. Preface

This chapter is concerned with a literature review of the study in hand. After a brief look into some important material requirements for photovoltaic applications, the properties of CdS and CdTe are discussed on the basis of their suitability for solar cell applications. In addition, published data on CdS/CdTe heterojunction cells are reviewed followed by a brief survey of other CdTe based cells.

3.2. Material Requirements for Optimum Solar Cells

The following properties, some of which are interrelated, are important for consideration for the choice of a solar material:

(1) Energy gap:

The energy gap of an absorber material places an upper limit on the wavelength of the incident radiation. The smaller the energy gap, the larger the portion of the solar spectrum which is potentially utilized, and therefore the greater the short circuit current. However, the maximum photovoltage attainable is correspondingly small. On the other hand, a large energy gap can give rise to high V_{oc} with lower leakage across the junction, but with lower I_{sc}. Therefore a judicious compromise has to be made to optimise the spectral response of the device. As a result of the non-smoothness of the solar spectrum [1], there have been a number of studies attempting to match the energy gap to the solar spectrum [2-5]. Figure 3.1 shows the maximum achievable efficiency as a function of

absorber energy gap for different window materials. These results relate to AM1 conditions and do not include refinements such as grain size or lattice matching between the absorber and window layer, which can further affect the performance. The optimum value of the energy gap for terrestrial applications is 1.5 eV [2].

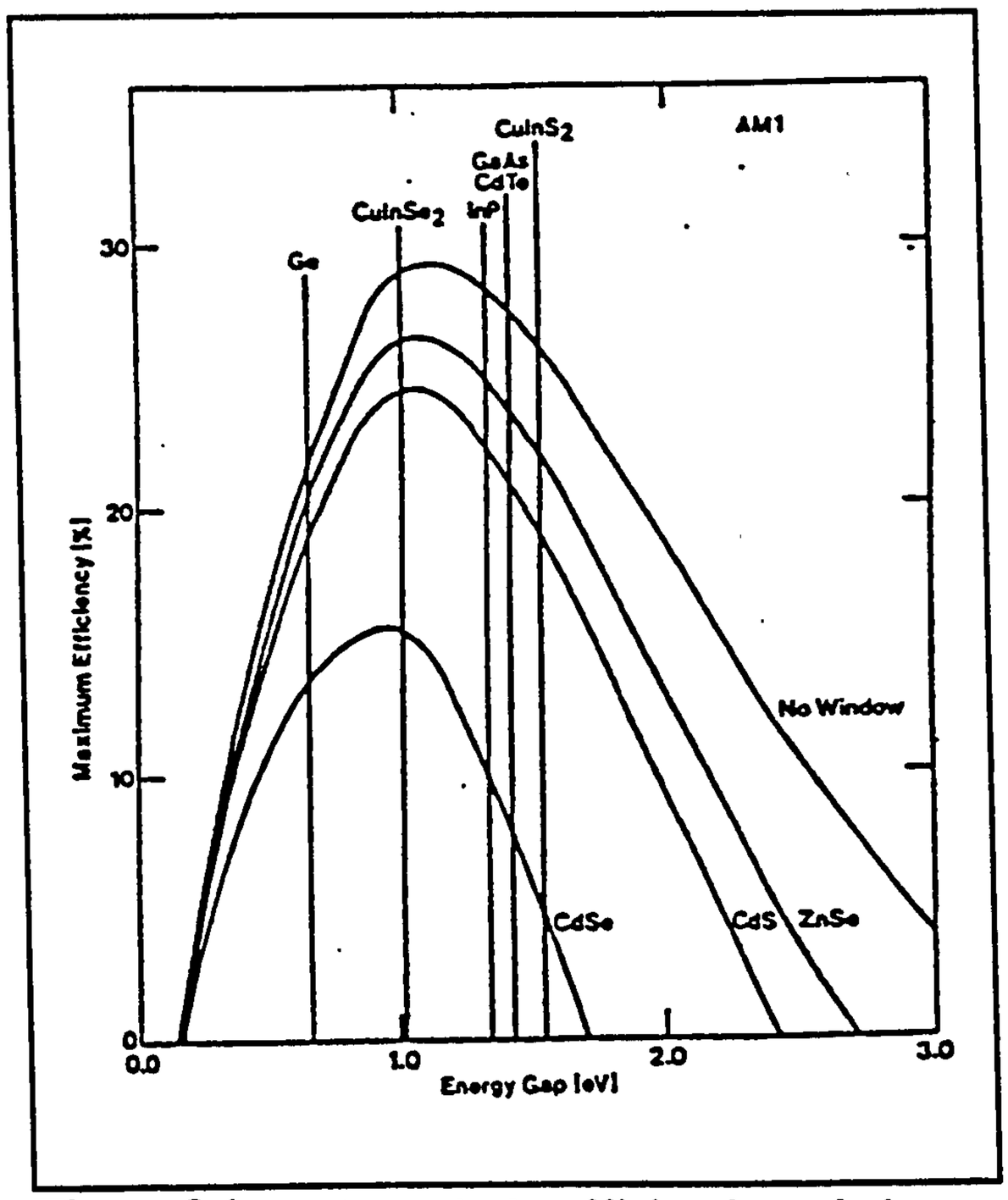

Figure 3.1 .. Theoretical efficiencies of hetero-junctionsolar cells as a functionof energy gap and window material [ref 6].

(2) Absorption coefficient:

In general absorber-generators should have large absorption coefficients (α) associated with interband transitions [7]. Since the necessary absorber thickness is of the order of $1/\alpha$ [6], a large absorption coefficient permits the absorber layer to be thin and hence less material is necessary for device fabrication. In principle, a direct bandgap material is more desirable, since the absorption coefficient is larger. Figure 3.2 represents the absorption coefficients of a function of photon energy for several solar cell materials.

(3) Diffusion length:

An essential requirement for the successful operation of a solar cell is that the photogenerated carriers must be able to move across the

absorption region to the junction. The charge carriers that recombine before arriving at the junction are lost to the photovoltaic effect and cannot contribute to the photocurrent. In general the diffusion length should also be of the order of $1/\alpha$ [6]. The diffusion length depends of various factors such as the impurity and defect concentration, the crystallinity of the material, the crystal orientation, and the stoichiometry.

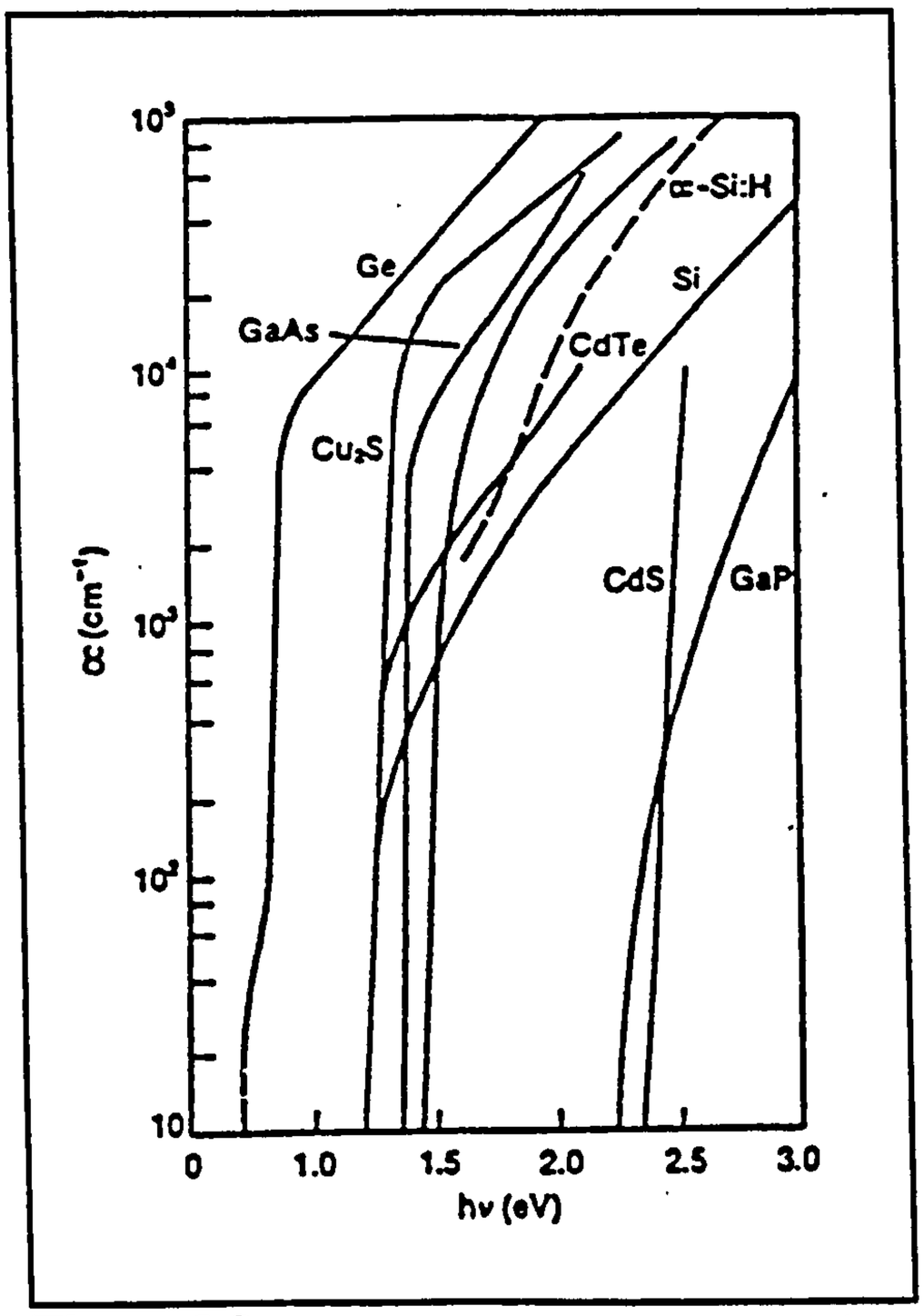

Figure 3.2 .. Optical absorption coefficient as a function of photon energy for several solar cell materials [ref 6].

(4) Minority carrier lifetime:

Large values of minority carrier lifetime are usually desirable for efficient devices. One factor which seriously reduces lifetime is the presence of a high density of localised states and in particular of the "killer" (recombination) centres located at the middle of the bandgap.

(5) Doping:

Impurity concentration levels can have a profound effect on absorption, diffusion length and energy bandgap [8]. It is desirable to obtain a large photovoltage and this requires high levels of doping. On the other hand, long lifetimes are also necessary and these are reduced by doping too heavily. It is also important that the series resistance of the cell be very small to reduce the ohmic losses in the device itself. These conflicting requirements necessitate that the doping level can be controlled

for optimum performance.

(6) Surface recombination and density of localized states:

Since carrier generation is highest at the surface and decreases exponentially with depth into the material, surface recombination can seriously limit photovoltaic device performance. High surface recombination arises from a number of causes including the presence of surface states associated with dangling bonds, native oxide layers, chemical residues, etc. Its effects can be reduced by various techniques for surface preparation or through passivation of the photovoltaic material surface. On the other hand, a high density of localized states results in extremely poor diffusion lengths. It is also difficult to dope materials effectively to form the necessary junction and obtain reasonable minority carrier lifetimes if the localized defect state density is high. This is especially critical for amorphous materials.

3.3. CdTe and CdS Semiconductors

In the previous section, there are clear indications that CdTe and CdS are good candidates to form an efficient solar cell. However, this section gives further details of their semiconductor properties.

3.3.1. Cadmium Telluride

Several extensive reviews of the properties of CdTe have been published [9-11]. Cadmium telluride is the only, II-VI compound with any promise to form a homojunction solar cell, since it can be prepared with relatively high conductivity in both n and p type forms. However, it is difficult to obtain very low p-type resistivity ($p > 10^{17}$ cm^{-3}) probably because of self compensation.

Among the more promising absorber materials CdTe has the largest

bandgap. It has a direct bandgap of 1.47 eV, close to the optimum of 1.5 eV for photovoltaic conversion of solar energy [3]. As a result, it was nominated as early as 1956 [12] as a possible candidate for a solar cell material. Its potential in heterojunction solar cells lies in its ability to develop a larger V_{oc} under illumination than can be achieved with cells made from smaller bandgap semiconductors. This offsets the decrease in I_{sc}, which is an inevitable consequence of its large bandgap.

CdTe has the advantage of a high optical absorption coefficient (~10^4 cm^{-1} at the band edge [13,14]). This means that photons with energies equal or greater than the bandgap are absorbed within a few (<5 μm) micrometres of the CdTe surface, and in principle, therefore less material is required for device fabrication. When used in a heterojunction photovoltaic cell with a suitable window material, photocarriers in the CdTe absorber are generated near the junction where charge separation and collection occurs. The requirement for large diffusion lengths (which are generally difficult to achieve in polycrystalline films) in the bulk is then relaxed. A high absorption coefficient thus has the advantage of a potential saving in the cost of the device, in comparison with Si (which has an indirect bandgap of 1.11 eV), where a layer of twenty microns thick is required to absorb the same proportion of light that is absorbed in less than 5 microns of CdTe.

Despite these fundamental attributes the full potential of CdTe for photovoltaic applications has not yet been realised because of inherent problems with the doping of the material. These problems have adverse effects on the minority carrier lifetime, resistivity, and ohmic contacts.

For efficient photovoltaic devices long lifetimes of minority carriers are desirable. It has been shown [15] that lifetimes of 10^{-7} sec in CdTe are essential to obtain a 10% efficient solar cell. However, minority carrier lifetimes in n-CdTe are generally less than 10^{-8} sec, and lifetimes are even shorter in p-CdTe [16,17]. Low minority carrier lifetimes are believed to be due to the presence of "killer"

centres near the middle of the bandgap. Bell et al [15] have also shown that lifetimes are affected by the chemical nature of the dopant. The search to find a suitable dopant to satisfy this requirement is still continuing.

Bulk resistivity of the semiconductor materials plays a crucial part in the photovoltaic conversion process, since a high series resistance leads to a substantial reduction in the solar cell output. The optimum CdTe resistivity for solar cell applications is thought to be in the range of 1-10 Ωcm [18]. Nevertheless, it would be better to obtain the lowest resistivity possible, because the depletion region and the minority carrier diffusion length would then be reduced causing both output current and voltage to increase. However, such low resistive p-CdTe is rather difficult to achieve, requiring carrier densities in the range of 10^{17}-10^{18} cm^{-3}. The work described in this thesis describes attempts to achieve low resistivity p-type CdTe by doping with phosphorus.

Low resistance ohmic contacts to the semiconductor layers are important basic requirements for the production of high efficiency solar cells. The work function of CdTe is 5.9 eV [19]. Theoretically, a barrier free contact to a p-type semiconductor is obtained when the work function of the metal used for the contact is greater than the work function of the semiconductor. Unfortunately, none of the commonly available metals has a work function large enough to match the work function of p-CdTe, and so it is always difficult to make ohmic contacts to the semiconductor. This problem will be discussed in detail in chapter eight.

3.3.2. Cadmium Sulphide

CdS is a natural choice as a window material in n-CdS/p-CdTe solar cells. Owing to its direct wide bandgap (2.4 eV), most of the incident solar spectrum will be transmitted. Moreover, as a consequence of the good match in electron affinities (˜4.5 eV [20]), the conduction bands of the CdS and CdTe join smoothly

at the interface [21-23]. CdS can only be doped n-type, nevertheless, it may be made highly conductive. This makes it possible to displace the region of maximum photocarrier generation away from the surface where the recombination velocity is very high into the region of maximum carrier collection.

Although the minimum melting temperature for CdS is 1475°C (accompanied by an equilibrium vapour pressure of ~4 atmospheres [24]), it sublimes readily at a much lower temperature of 700°C , so that it can be evaporated to form thin films. Unfortunately, there is a relatively large lattice mismatch between CdS and CdTe, and moreover, CdS generally crystallizes in the hexagonal wurtzite structure whereas CdTe is cubic. Consequently, CdS deposited on CdTe is usually polycrystalline, although epitaxial growth on certain crystallographic plans of CdTe is possible [25-27].

For heterojunction solar cell applications, it is known that higher J_{sc} and higher efficiencies can be achieved by reducing window layer absorption. In CdS/CdTe cells, this is accomplished by reducing the CdS thickness (values of J_{sc} greater than 24 mA/cm^2 were reported for CdS films with thicknesses less than 0.2 μm) [28,29]. Nevertheless, CdS and CdTe interdiffusion increasingly becomes more likely to occur as CdS thickness decreases [30,31]. Wilson and Woods [32] observed a dependence of resistivity on thickness which was explained in terms of an increasing deviation from stoichiometry of the source material as the CdS evaporation proceeds. This was latter observed also in CdS [33] grown by spray pyrolysis.

Cadmium sulfide has been widely and successfully used as a window material in many systems. The CdS/Cu_2S heterojunction is perhaps the most extensively researched device. Thin film cells of Cu_2S/CdS with active area of 1 cm^2 and efficiencies up to 9% have often been described [34], and high efficiencies of 17% with InP/CdS [35], have also been reported. Besides CdTe, $CuInSe_2$ is one of the most promising partners of CdS involved solar cells. The

best $CuInSe_2$/CdS device has an efficiency of 14.1% [88].

An important consideration from an economic point of view is that CdS is comparably inexpensive and good quality thin films are producible using relatively inexpensive techniques such as evaporation, screen printing and r.f.sputtering.

3.4. CdTe Based Solar Cells

The history of CdTe solar cells dates back to the 1960s when Vodakov et al [36] and Naumov and Nikolaeva [37] reported efficiencies of 4 and 6 percent respectively for their homojunction cells. However other early studies of cadmium telluride revealed that an economical CdTe homojunction terrestrial cell was not feasible, because minority carrier lifetimes in CdTe were less then 10^{-8} sec [16,17,38]. Nevertheless, Barbe et al [39] produced a shallow homojunction cell on an n-type substrate with an efficiency of 13% under AM1 illumination.

Because of the short optical absorption length in CdTe and the difficulty of forming a thin film shallow junction with a high conductivity surface layer, it is much preferable to form solar cells with the heterojunction configuration, where a transparent conducting semiconductor is used as the partner. Several CdTe heterojunction cells have been fabricated and investigated during the last two decades in attempts to produce an efficient cell. Reviews of CdTe based solar cells may be found in [40-43].

3.4.1. CdS/CdTe Solar Cells

Preliminary results with CdS/CdTe cells were reported in 1964 by Muller and Zuleeg [44], who deposited 1μm thick film of CdS by vacuum evaporation on 500A° CdTe layers to form a structure of Al/CdS/CdTe/Au. Four years later, Dutton and Muller [45] reported cells formed by evaporating ~100A° of either Te

or CdTe onto ~1μm thick films of CdS. However, spectral sensitivity studies revealed the presence of a CdS_xTe_{1-x}graded region at the interface, indicating that these devices were not ideal heterojunctions. In 1971, Bonnet and Rabenhorst [46] produced CdS/CdTe heterodiodes with graded bandgaps by co-evaporation of CdS and CdTe onto glass substrates maintained at 180°C.

In the early 1970's, growing interest in CdS/CdTe devices was diverted towards fabrication and evaluation of thin film diode arrays [47-49] for applications in optoelectronics. For the layer structure of n-SnO_2/n-CdS/p-CdTe/metal, the photovoltaic parameters under an illumination with 100 mW/cm^2 were 0.3V for the open circuit voltage and 15 mA/cm^2 for the short circuit current. The spectral sensitivity of the photovoltage was consistent with the known cut-off wavelengths for CdS and CdTe.

In 1975 Yamaguchi et al [25] produced a single crystal CdTe/CdS cell with an efficiency of 4.5%, an open circuit voltage of 0.55V, a short circuit current of 14 mA/cm^2 and a fill factor of 47%. The cells were fabricated by vapour deposition of In-doped CdS onto P-doped CdTe substrates in a H_2 atmosphere at a substrate temperature of 400 to 500°C. The CdS layer was about 300 μm thick with a resistivity of 0.1 Ωcm. SEM studies of the junction indicated the diffusion of indium into the CdTe to form an n-CdS/n-CdTe/p-CdTe junction. After further development, Yamaguchi et al [26] obtained an active area efficiency of 12% in cells fabricated by epitaxial growth of CdS on {111} face P-doped CdTe grown by the Bridgman technique. A year later they [50] calculated a theoretical efficiency of an epitaxial n-CdS/p-CdTe cell as approaching 20%. They described a basic structure of In-Ga/CdS/CdTe/Ni [26]. Careful analysis of this cell indicated that it was actually a buried homojunction with an n-CdS/n-CdTe/p-CdTe structure. Bube et al [51] have also produced 7.9% efficient devices using the same approach.

An early consideration of the problem of forming ohmic contacts to p-

CdTe was given in 1972 by Bonnet and Rabennhorst [52]. They found that it was necessary to use a thin layer of Cu to enhance the ohmicity of the back contact to p-CdTe. In their experimental arrangement, a thin layer of Cu was first evaporated onto a molybdenum foil substrate, this was followed by deposition of a layer of 10-20μm thick CdTe using a high temperature reactor, then a layer of CdS was vacuum evaporated at a substrate temperature of 180°C. Two years later Fahrenbruch et al [53] used In and Ni to make ohmic contacts to CdS and CdTe respectively. They deposited CdTe onto a single crystal CdS using a close-space vapour transport method in H_2. They obtained an open circuit voltage of 0.61 V, a short circuit current of 14 mA/cm^2 and a fill factor of 36% under 80 mW/cm^2 illumination. The highest efficiency they achieved at that time was 4%, although they calculated the theoretical efficiency to be 17% [53].

A 10.5% efficient solar cell was reported in 1982 by Tyan and Perez-Albuerne [54]. In their paper they described a thin film heterojunction fabricated by a close-space sublimation technique. The cells had typical values of open circuit voltage of 0.75V, short circuit current 17 mA/cm^2, with a fill factor ˜62% under simulated AM2 illumination.

Several other CdS deposition methods were applied in device fabrication. Fahrenbruch et al [55] used spray pyrolysis to put down windows of CdS and ZnCdS on CdTe wafers to produce CdS/CdTe and ZnCdS/CdTe heterojunctions. These cells exhibited efficiencies of 6.0 and 7.8% respectively. Electrodeposition was also used to fabricate CdS/CdTe solar cells [56]. The efficiency achieved was 8% for small area (0.02 cm^2) devices and 7% for large areas (4.2 cm^2) under 80 mW/cm^2 illumination. A 12.8% efficient CdS/CdTe solar cell was achieved using screen printing [57] methods. S.Ikegami was the first to report CdS/CdTe solar cells fabricated by a screen-printing-sintering-technique [58]. Other techniques for CdS thin film deposition have been investigated, such as electroplating [59], close-space sublimation [54], chemical vapour deposition [50] and pulsed laser driven

physical vapour deposition [60]. New methods are being developed for large area deposition of CdS films, a recent one known as the writing method [61], has been developed by the Matsushita Battery Industrial Co.

Because of the different crystal structures in the two compounds crystalline, epitaxial CdS/CdTe heterojunctions are not generally regarded as being possible. Deposition onto low index planes (eg {100},{110}) of CdTe always yielded polycrystalline layers, but when the CdS was grown specifically onto {111} [26,27,62] or {221} orientations, epilayers of good quality resulted [27,62].

Currently, the CdS/CdTe heterojunction is of interest as a potentially low cost thin film solar cell [63,88]. Detailed studies of the fundamentals behind heterojunction operation and production of large area thin film cells have received special consideration in recent years. C.Ercelebi et al [64] investigated current transport mechanisms in epitaxial CdS/CdTe cells. They found that the current transport across the junction is dominated by a multi-step tunneling/recombination process. Other workers [65,66] have come to the same conclusion.

Conversion efficiencies of higher than 10% have been reported for thin film CdS/CdTe solar cells [41,67,68].The highest efficiency, yet, reported was achieved by T.Chu et al [69]. Using an antireflection coating and a thin film structure of SnO_2/CdS/CdTe/graphite, they managed to obtain a 14.6% efficiency. Under global AM1.5 conditions and for a 1 cm^2 total conversion area, the photovoltaic parameters were; 0.805 V for the open circuit voltage, 24.4 mA/cm^2 for the short circuit current density, with a fill factor of 70.5%. For large scale cells, the BP research [29] team have reported recently a 9.5% efficient cell for a 3×3 cm^2 series inter connected CdTe solar cell, which the highest reported efficiency for such large area cells. For small area devices, they have reported a 13% efficient CdS/CdTe cell based on electrodeposited CdTe [29].

After being prepared in high conversion efficiency, CdS/CdTe solar cell

stability becomes an important consideration. Several reports indicate that thin film CdTe cells exhibit stable behaviour [70,71]. Nevertheless, one major problem with CdS/CdTe solar cells is the lack of a satisfactory ohmic contact to p-CdTe [72].

A recent recalculation of the theoretical efficiency of CdS/CdTe cells predicted a 27% of efficiency [73], while the practically achievable efficiency should be ~22% [74]. It was suggested that the cross-over of light and dark I-V behaviour, higher recombination current under light, large ideality factor, extraneous states and interdiffusion between CdTe and CdS materials are potential efficiency limiting mechanisms in CdTe/CdS devices [73,74]. However, physical defects responsible for the above defects have either not been identified or understood to the point that further improvements in efficiency can be achieved systematically and scientifically. An ongoing race is taking place to tackle this subject, an example of which may be found in ref [75].

3.4.2. Other CdTe Based Solar Cells

Cadmium telluride has been used in several heterojunction photovoltaic cell structures. In 1963 Cusano [76] produced CdTe/Cu_2Te thin film and single crystal heterojunctions with efficiencies of 6 and 7.5% respectively. The cells were fabricated by treating CdTe films and single crystals in a warm aqueous solution of cuprous chloride to form copper telluride. Similar devices were prepared by Leburn [77] and Bernard et al [78] using flash evaporation of Cu_2Te although this was never fully investigated.

The use of a larger bandgap window in place of CdS should in principle result in more efficient cells. One possibility is the use of indium tin oxide (ITO). Early results showed higher values of open circuit voltage as expected [51]. A solar efficiency of 10.5% (calculated for the active area) was achieved with V_{oc}=0.85 V and I_{sc}=20 mA/cm^2 for p-type single crystal CdTe substrate cells, and

5.5% for thin film ITO/CdTe cells. A few years latter, Werthen et al [79] reported a 10% efficient cell of the same structure fabricated by electron-beam evaporation of ITO onto p-type single crystal CdTe. T.Nakazawa et al [80] reported a 13.4% efficient cells with the same structure. Their investigation suggested the existence of a buried homojunction structure.

Other wide gap semiconductors have also been studied. Zinc oxide (E_g= 3.3 eV) has been investigated as a possible window material for p-CdTe solar cells. Using spray pyrolysis, J.Aranovich [81] achieved 8.8% efficient cells by depositing ZnO film onto 1 Ωcm resistive p-CdTe single crystal dice. Previous work in Durham has produced cells with conversion efficiencies of 6% [82] using the same approach with In doped ZnO. ZnO films have also been deposited onto single crystal CdTe using other techniques such as evaporation [83] and RF sputtering [84], where the conversion efficiencies did not exceed 4.8%. Thin film based ZnO/CdTe cells were produced by M.S.Tomar [85] with maximum efficiency of 3.7%. ZnSe/CdTe cells have also been considered but low efficiencies (1-2%) were the result [86].

K.W.Mitchell et al [87] fabricated a 10.5% efficient thin film CdTe based solar cell in a completely non-vacuum process and with tin oxide as the window layer. Using a close-space vapour transport (CSVT) method, they deposited a 4 cm^2 CdTe film onto a wide band gap conductive layer of tin oxide, and used screen printed C-Au for the back contact. Under a 100 mW/cm^2 air mass 1.5 global spectrum, a short circuit current of 28.1 mA/cm^2, an open circuit voltage of 0.663 V and a fill factor of 0.563 were measured.

Clearly, cadmium telluride based solar cells have offered considerable promise during the last two decades, nevertheless, the efficiencies achieved are still well below the theoretical maximum. Much research still remains to be done before the full potential of the material can be realized.

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Chapter IV

Material Preparation Techniques

4.1. Preface

The work presented in this thesis relates to the study of CdS (thin film)/CdTe:P (bulk crystal) photovoltaic devices. This chapter is therefore devoted to a description of the techniques employed in the fabrication of the device in a variety of structures. Almost all of the starting materials used in this work were prepared in house, and hence the chapter will flow from the very formation of the compounds to the final stages of device preparation . It is concerned with material preparation and bulk/layer growth. In addition to surface treatments, two methods of controlling the resistivity (doping) of p-CdTe are discussed, as is the approach used to form ohmic contacts with the resulting material. Finally, it is shown how In/CdTe Schottky diodes and CdS/CdTe solar cells were fabricated.

The author is indebted to Mr. N.F.Thompson for growing the CdTe crystals used in the doping study, and Mr. M.Bayhan for depositing the CdS thin films used in device fabrication.

4.2. Materials Preparation

The CdTe starting material for the growth of bulk crystals was synthesised in this laboratory by direct combination of high purity double zone refined cadmium and tellurium (both 'six 9' purity) supplied by M.C.P. Electronic Materials Ltd. A charge of cadmium and tellurium in stoichiometric proportions was loaded into a silica tube sealed at one end. The tube was evacuated to a pressure of $\sim 10^{-6}$ mbar and left to outgas for 24 hours. The tube was then sealed

using an oxy-acetylene gas torch and placed in a furnace. The furnace temperature was increased slowly to 940°C over a period of a few hours and thereafter maintained at that temperature for 3 days. The charge was cooled down slowly over several hours. This produced a solid lump of CdTe which was then crushed mechanically and used as the source material for the preparation of bulk crystals.

The CdS material employed was supplied by G.E.America. Commercially available CdS is known to contain trace amounts of both volatile and non-volatile impurities. These impurities can seriously affect the opto-electronic properties of the material and of devices fabricated from it. It was therefore necessary to purify the source material, before it was used for the deposition of thin films. Consequently, it was purified by sublimation in an argon flow-run process. A small quantity of CdS was placed in a silica boat and loaded at one end of a silica tube next to a two silica liners. This assembly was then placed in a furnace with one end of the tube connected to the exhaust. The tube was first flushed with argon for one hour and then heated to 600°C for six hours to drive off the volatile impurities from the charge. The furnace temperature was then raised to 1160°C while maintaining the argon flow. The charge was then transported from the source boat (where sublimation was occurring) to the liners in the cooler part of the furnace. Needles and platelets of yellow CdS formed on the walls of the first liner, while most of the more volatile impurities and CdS that had failed to condense on the walls of the first liner were collected on the second liner. Non-volatile impurities such as Zn, Fe, and Mn, were left in the residue of the charge. The CdS platelets deposited in the first liner were removed from the silica but the first layer attached to the liner was not removed as it may have contained impurities that had diffused out of the silica.

4.3. CdTe Crystal Growth

There are three general approaches to the growth of CdTe bulk crystals. The most widely used method is to grow the crystal from congruent melts using Bridgman and Vertical Zone Refining Techniques. These methods are capable of producing large single crystals [1] at relatively high growth rates. In addition, the crystal grower has greater freedom to control the type of conductivity of the crystals. However, because of the high temperatures involved, contamination from the quartz crucible is possible, and thus lower temperature methods of growth from Te-rich solutions have been investigated. Alternatively, the crystals may be grown from the vapour phase at lower temperature thus avoiding contamination associated with the high temperature Bridgman growth. Crystals grown from the vapour phase have been shown to be of comparable perfection and purity [2,3].

The cadmium telluride crystals used in the present study were grown in our laboratory by a vapour phase technique originally developed by Clark and Woods [4] for CdS and adapted for CdTe. A specially designed growth tube fabricated to our specification by Heraeus Ltd. was used to grow the crystals. In essence, this consisted of a silica capsule in which was fitted a conical growth tip, a small bore tube formed the "tail". The function of the latter was to provide some control of the constituent partial pressures during growth.

A measured quantity of synthesized polycrystalline charge of the CdTe, prepared as in section 4.2, was loaded into the growth capsule and appropriate amount of Te was placed in the tail to enhance the growth [3]. The tube was then evacuated to a pressure of ~10^{-6} mbar and allowed to outgas for 24 hours. After this, the tube was sealed under vacuum. The sealed tube was suspended vertically in a double zone furnace as shown in figure 4.1. Initially the tube was placed in the furnace with the growth tip at the highest temperature, to sublime any CdTe debris away from the growth tip before growth began. The tube was then pulled through the furnace at a rate of 15 mm per day, until a temperature gradient of

50°C was established between the charge and the growth tip. The pulling was then stopped and the tube allowed to remain in this position for seven days. Finally the temperature of the main furnace was gradually reduced to room temperature over ~3 days. The reservoir furnace, which was independently controlled was switched off when the temperature of the main furnace had fallen to that of the reservoir. With this technique, CdTe boules ~29 mm in diameter and 5 cm long could be grown from a charge of 150 gram.

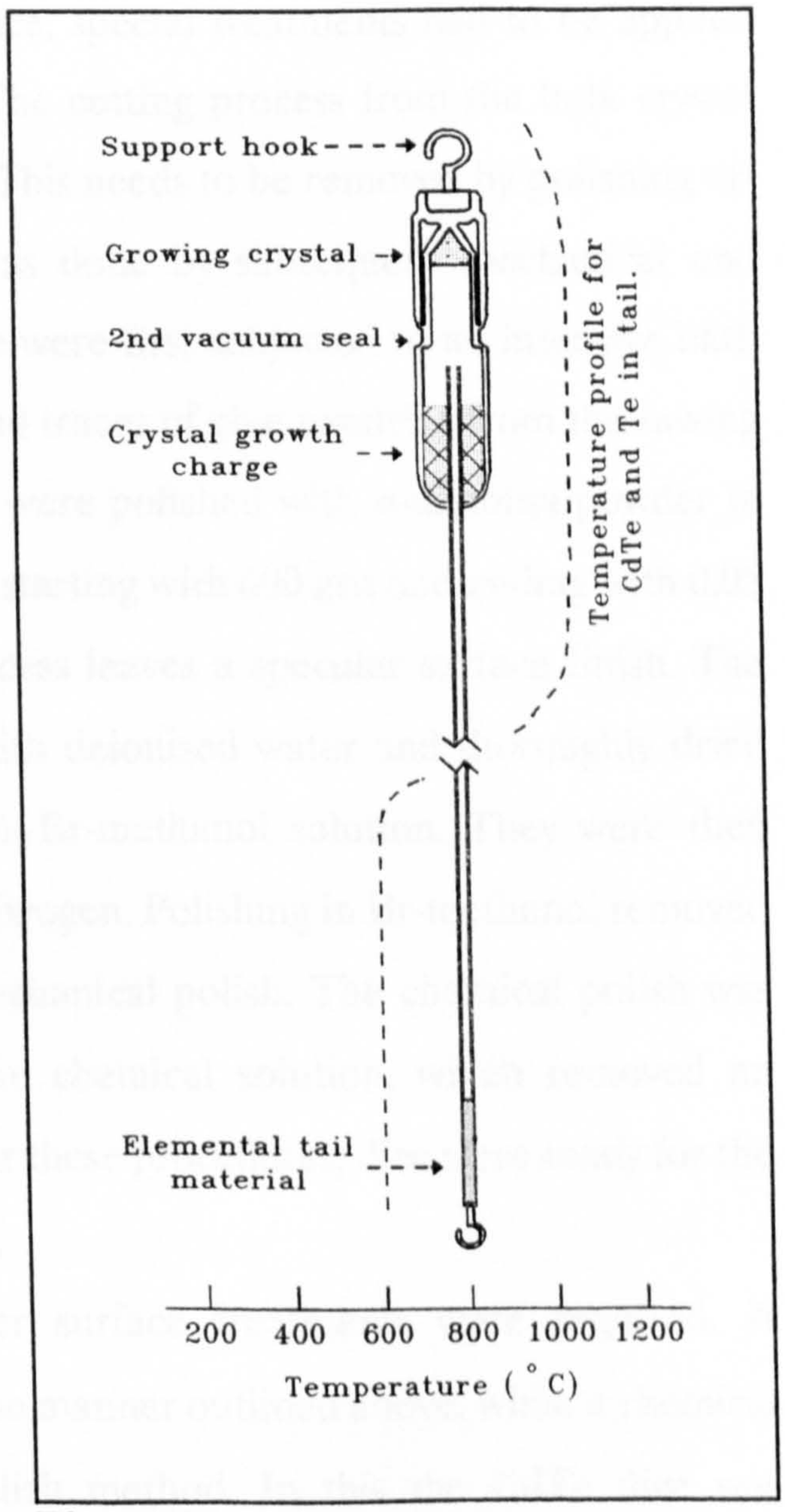

Figure 4.1 .. The growth capsule as it hangs in the furnace with the temperature profile across the vessel.

4.4. Sample Orientation and Preparation

For CdS/CdTe solar cell fabrication it is desired to use clean {111} face surfaces. It was necessary therefore to subject the CdTe crystals to preliminary preparation processes. Grown boules usually contain many single crystals in different orientations. After a fast HF etch, the single crystals in the grown boule become more obvious to the naked eye, where the biggest crystal was then identified and oriented for the {111} direction using the Laue x-ray method. After identifying the desired orientation, the boule was sliced to a thickness of 1.8-1.2 mm using a diamond saw. The slices were further

cut into small dice with dimensions of 5 × 5 mm^2. Single crystal dice were then subjected to special surface preparation procedures before and after the resistivity control process and before p-n junction formation.

Because the quality of the substrate surface is an important factor in determining the final device performance, special treatments had to be applied to achieve the desired surface finish. The cutting process from the bulk crystal leaves saw damage on the free surface. This needs to be removed by polishing off a certain amount of material. This was done by subsequent mechanical and chemical treatments. However, the dice were first subjected to an intensive bath in acetone in order to remove grease and traces of glue resulting from the sawing process. For the mechanical part, dice were polished with α-alumina powder in a decreasing sequence of particle sizes, starting with 600 grit and ending with 0.05 μm particle size in 4-5 steps. This process leaves a specular surface finish. The polished samples were then washed with deionised water and thoroughly dried before being etched chemically in 2% Br-methanol solution. They were then rinsed in methanol and blow-dried in nitrogen. Polishing in Br-methanol removed the work damage produced by the mechanical polish. The chemical polish was carried out by rinsing the dice in the chemical solution, which removed an average some 60 μm in 5 minutes. After these procedures, dice were ready for the resistivity control (doping) treatments.

After doping the dice, further surface treatments were required. A mechanical polish was carried out in the manner outlined above, while a chemical one was performed using a pad polish method. In this the CdTe dice was mounted using wax on the end of a PTFE shaft, which in turn was mounted (sliding fit) in a cylindrical housing. A PTFE/fiberglass pad was placed in the bottom of a circular trough containing the Br-methanol solution. Figure 4.2 illustrates the pad polish arrangement. A sample mounted on the shaft assembly could be polished rapidly with no downward pressure directed onto the CdTe

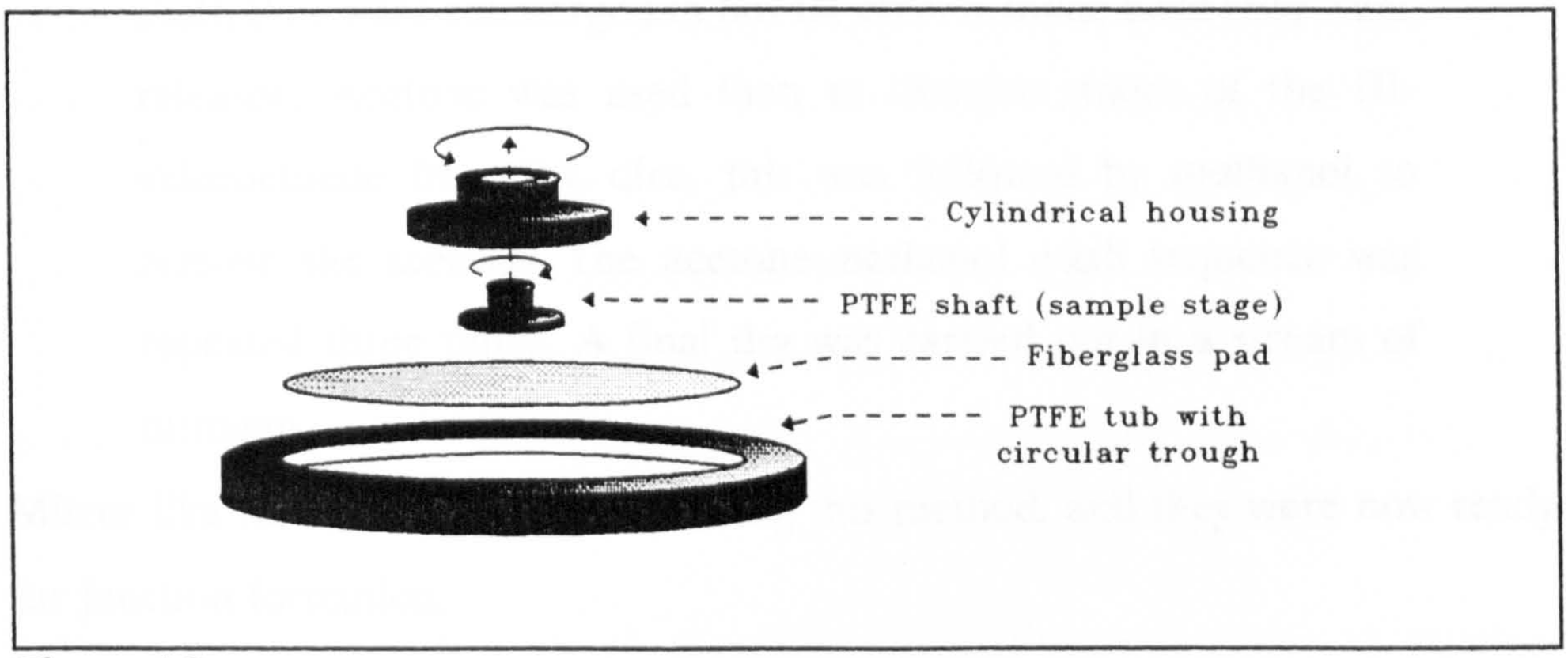

Figure 4.2 .. A schematic diagram of the Pad Polish arrangement, used for chemical etching of CdTe dice.

substrates other than from the weight of the PTFE shaft on which it was mounted. The method is close to a contactless polish, since this arrangement traps a very thin layer of Br-methanol solution between the substrate and the pad. With experience the following procedure was developed:

The CdTe substrates were first washed in acetone for a couple of hours, to remove grease and glue traces. To remove heavy saw damage the substrates were mechanically polished in the sequence 600 grit, 9.5 μm, 3 μm, 0.3 μm, then 0.05 μm (α-alumina particle size), this was carried out on specially reserved cotton buds (Q-tips) for each particle size, having washed the dice thoroughly in water after each stage. Dice were then washed in deionised water before being dried in an air-flow. A thorough methanol wash preceded the chemical treatment to remove water traces. Using wax, dice were then mounted onto the PTFE stage. Excess wax was removed from the upper surface and edges firstly with a fine knife, then by a fast hot III-chloroethene wipe. Having carried out the pad polish as outlined in the prior paragraph, the dice were given a complete methanol wash and dried in nitrogen. To release the dice from the

shaft, they were submerged in hot III-chloroethene until they were released. Acetone was used then to dissolve traces of the III-chloroethene from the dice, this was followed by methanol to remove the acetone. The acetone-methanol wash sequence was repeated three times. A final dry was carried out in a stream of nitrogen.

Mirror like surfaces were obtained using this method, and they were now ready for junction formation.

4.5. Single Crystal CdTe Doping Systems

Single crystal doping is usually performed during the growth process, however, such an approach proved unsuccessful in our method of growing CdTe crystals. This was because phosphorus, as the p-type dopant, was found to attack the growth tube resulting in disastrous consequences. Successful doping of CdTe was achieved using a post-growth doping (PGD) treatment. This approach consists of two stages; firstly the sample surface is coated with a thin layer of the required impurity, and secondly this impurity is driven into the bulk material.

The systems used in post-growth doping of the CdTe crystals are described in detail in the following section.

4.5.1. First Doping Stage

For this stage of the PGD process, two systems were investigated, described as the Open Tube Doping Method and the Sealed Tube Doping Method. Both methods were successful in reducing the bulk resistivity.

4.5.1.1. The Open Tube Doping Method

This method had previously been used in our laboratory where the lowest

resistivity of p-type CdTe produced was 100-125 Ωcm [5]. Further developments were made to the system, and the final arrangement is illustrated in figure 4.3. Here phosphorus from orthophosphoric acid was used as the impurity material for the p-type conversion of the bulk CdTe.

As the name implies, the exit end of the reaction tube is open to the outer atmosphere through vapour traps. CdTe dice, (grown as in section 4.3, and

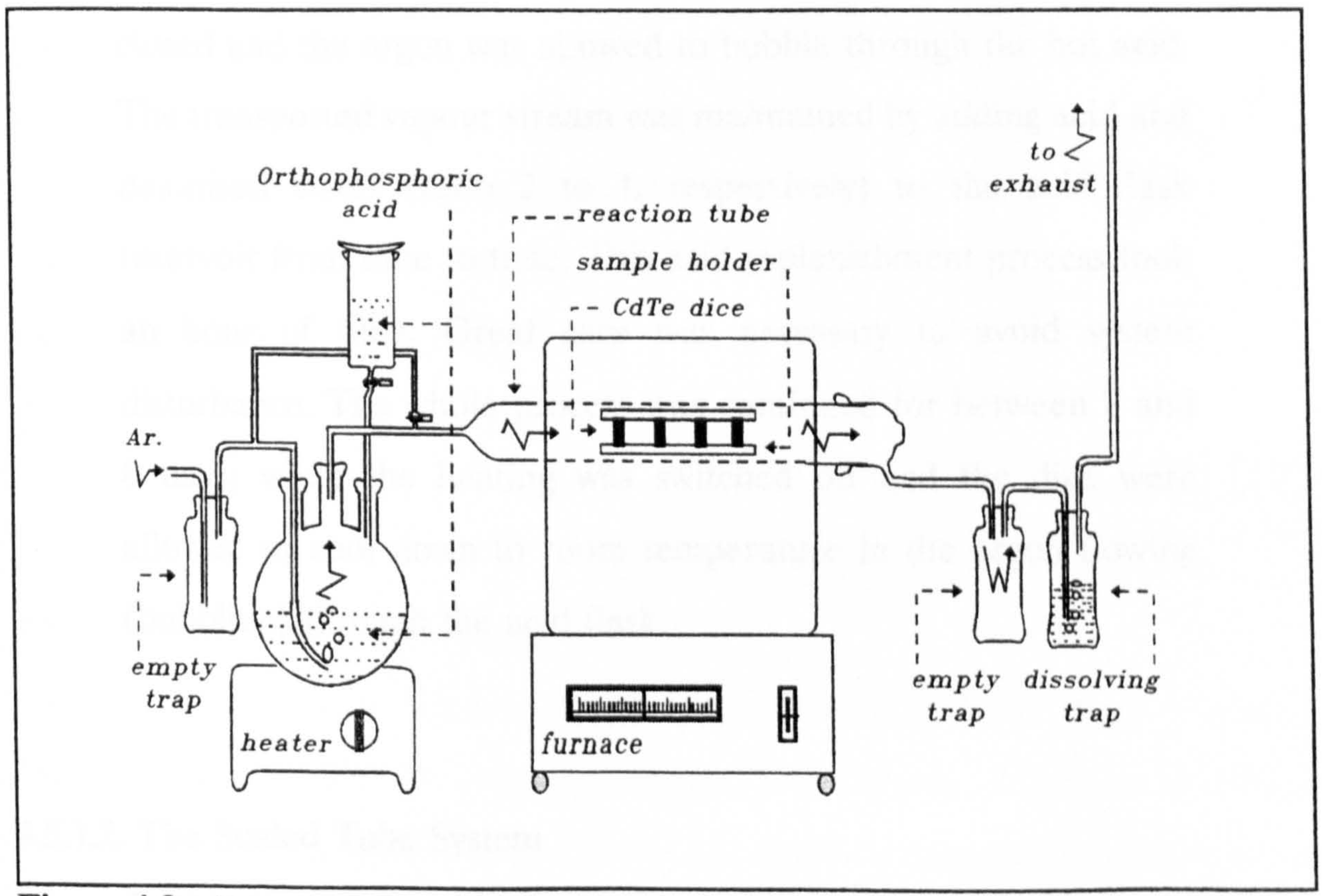

Figure 4.3 .. Experimental arrangement for post-growth phosphorus doping of CdTe.

prepared as described in section 4.4), were mounted in a silica holder and placed in a reaction tube in a furnace at temperatures between 280-600°C. The entry end of the tube was connected to a flask containing orthophosphoric acid, the acid was heated and maintained at 180-200°C. Argon passing through an empty trap and bubbling through the acid, was used as the vapour carrier gas. To prevent condensation the pipes between the flask and the reaction tube were wrapped with an insulating high temperature textile. The vapour at the exhaust was

condensed and collected in an empty cold trap, and any uncondensed vapour was dissolved in an NaOH trap. Several different dice holders were tried, the best results were achieved where most of the dice area was exposed to the vapour flow. Swage Lock PTFE connections were used to block any leakage. The procedure was as follows;

The reaction tube was first flushed with argon via a bypass line, while both the acid and the dice were heated each to the desired temperature. At stable temperature, the bypass line was closed and the argon was allowed to bubble through the hot acid. The transported vapour stream was maintained by adding acid and deionised water (ratio 2 to 1, respectively) to the acid flask reservoir from time to time. This acid replenishment process took an hour of time. Great care was necessary to avoid system disturbance. The whole process was continued for between 2 and 8 days; when the heating was switched off and the dice were allowed to cool down to room temperature in the argon flowing (bubbling) through the acid flask.

4.5.1.2. The Sealed Tube System

In this arrangement the impurity source and the CdTe dice were sealed together in a silica glass tube. To accomplish this, the CdTe dice (prepared as above) and orthophosphoric acid or other dopant source (further detailed in chapter 6) were sealed in silica ampoules formed with two compartments joined by a narrow neck. One compartment held the CdTe dice, the other a small quantity of the dopant source. The sealed tube arrangement is shown in figure 4.4. The tube was evacuated to 4×10^{-2} mbar. The ampoule was then sealed and placed in a vertical double zone temperature controlled furnace so that the CdTe

dice were at ~420°C and the acid reservoir was at ~200°C. The CdTe was suspended at the top. Vapour from the impurity source created a local source of impurity in the vicinity of the CdTe. This process was continued for periods of 1 to 11 days, when the heating of acid was switched off and the dice allowed to remain at higher temperature for a few hours before cooling to room temperature. This prevents acid from condensing around the dice in the cooling down period.

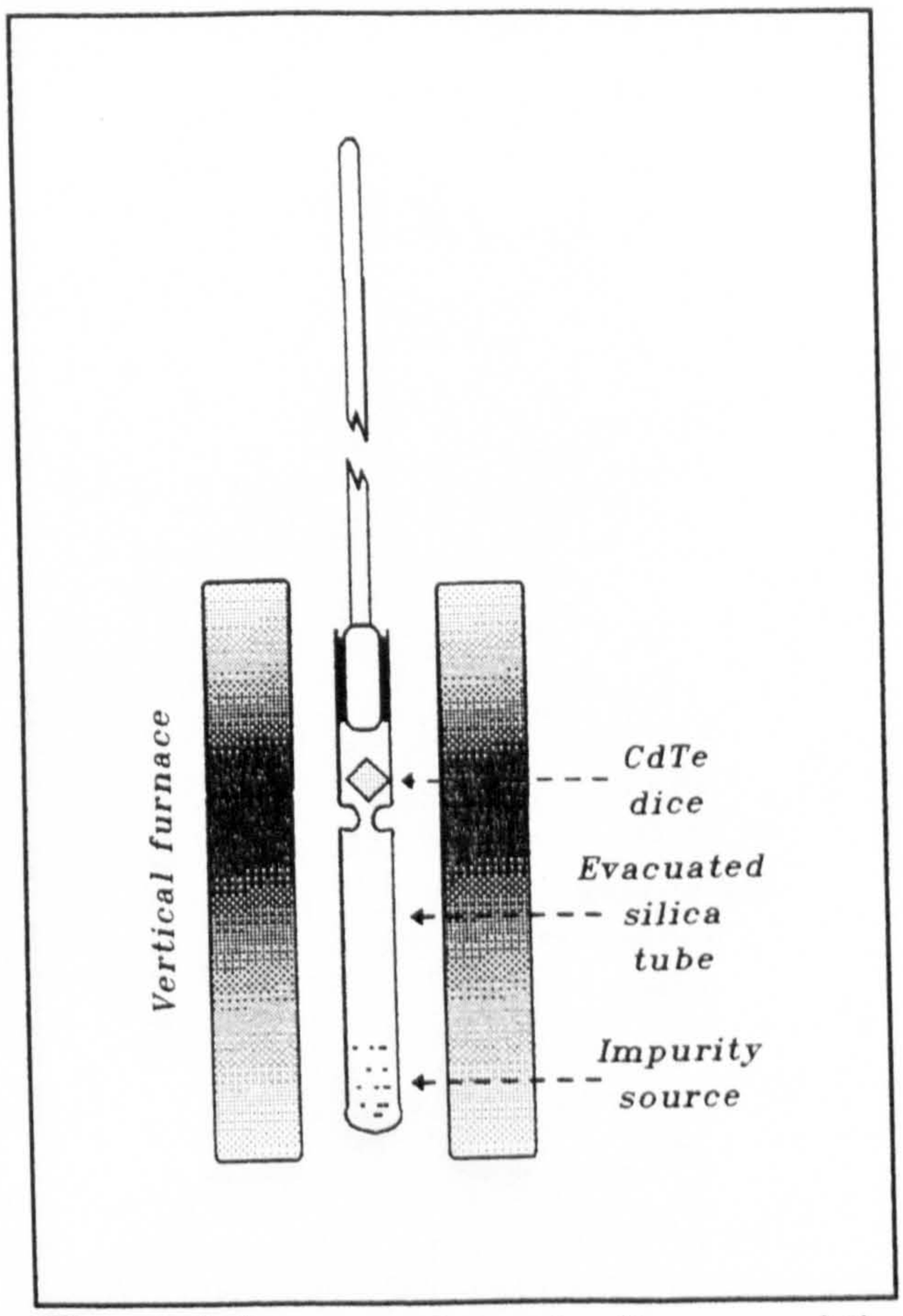

Figure 4.4 .. A schematic diagram of the sealed tube arrangement used in the first stage of the PGD treatment of CdTe.

4.5.2. Second Doping Stage; Annealing

Annealing is the drive-in process of the impurity atoms (P for instance) that were deposited in the first stage of the PGD process. When the first stage was completed (i.e. section 4.5.1.1 or 4.5.1.2) the dice were then annealed in an atmosphere of Te or Cd for periods of 3 to 9 days. To accomplish this, the P-doped dice were sealed in silica ampoules formed with two compartments joined by a narrow neck. One compartment held the CdTe dice, the other a few chips (3 mg) of Te (or Cd). This arrangement is illustrated in figure 4.5. The tube was evacuated to 2-3 × 10^{-5} mbar. The ampoule was then sealed and placed in a vertical temperature controlled furnace so that the CdTe dice were at ~550°C and the Te reservoir was at 410°C, once again the CdTe was suspended at the top. This prevented sublimation of the dice but allowed a Te vapour pressure to be

established around the CdTe dice. This vapour pressure aided annealing of the dice, promoted even phosphorus distribution throughout the dice, encouraged the reduction of Te vacancies, and possibly introduced interstitial Te atoms. Some or all of those processes could contribute to the reduction in resistivity of the bulk material.

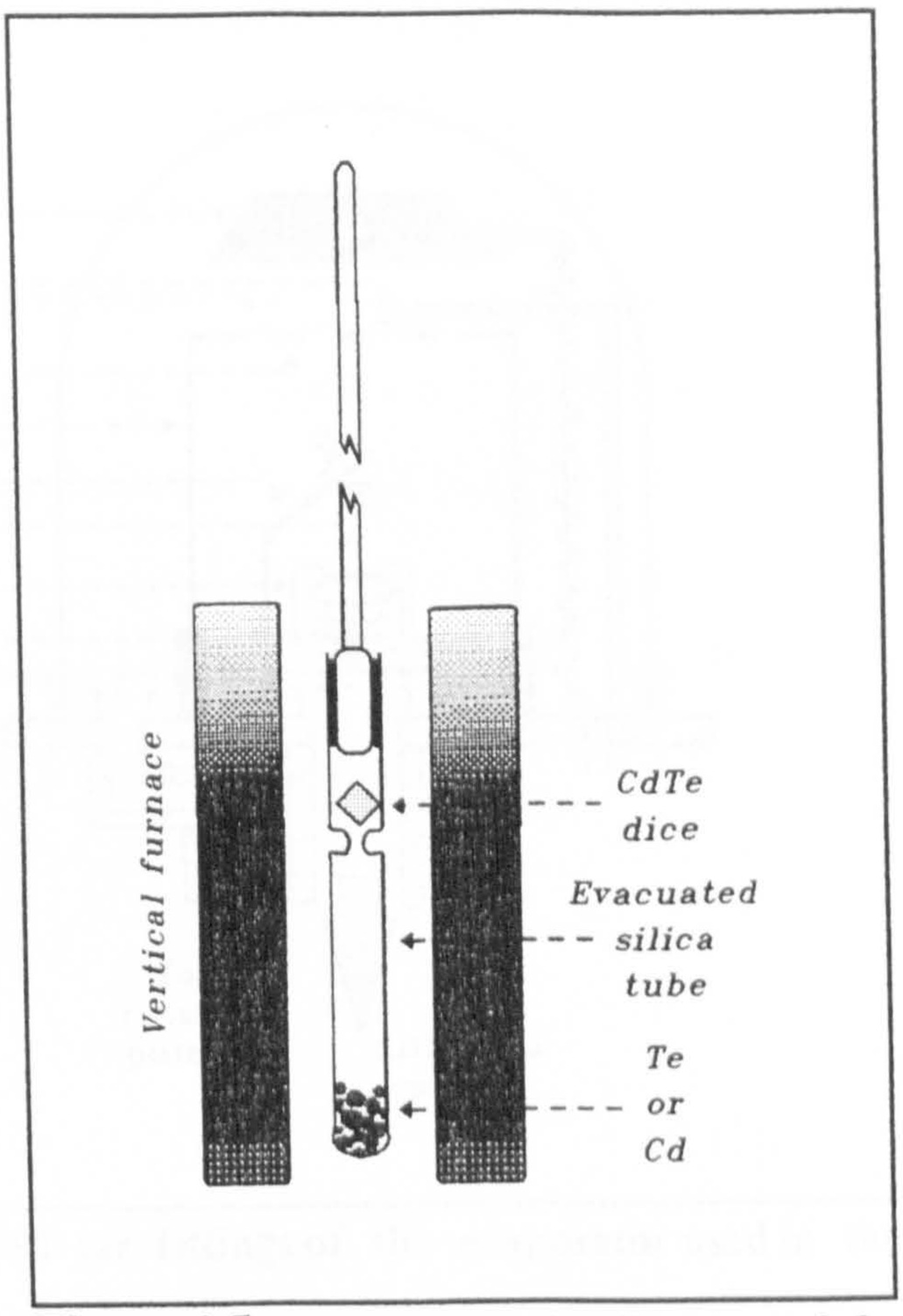

Figure 4.5 .. A schematic diagram of the sealed tube arrangement used in the second stage of the PGD treatment(annealing) of the CdTe.

4.6. CdS Deposition System

Although a large variety of deposition techniques (including thermal evaporation, spray pyrolysis, sputtering, screen printing and electrodeposition) have been exploited to prepare solar cells, it was decided that the cadmium sulphide films would be grown by conventional thermal evaporation. An inhouse built system, capable of achieving a pressure of ~10^{-7} mbar in the bell jar, was used. A schematic diagram of the bell jar fittings is shown in figure 4.6.

The substrates (CdTe:P) were heated by radiation from a 1000 W infrared lamp. The substrate temperature was controlled by a Eurotherm controller with a NiCr/NiAl thermocouple which was clamped to the back of the stainless steel substrates holder which carried the substrates with their stainless steel masks.

As undoped CdS films were used, a single resistively heated tantalum crucible provided the evaporation source. The charge temperature was measured using a Pt(13%)Rd/Pt thermocouple sealed in a silica tube with a sharp tip which

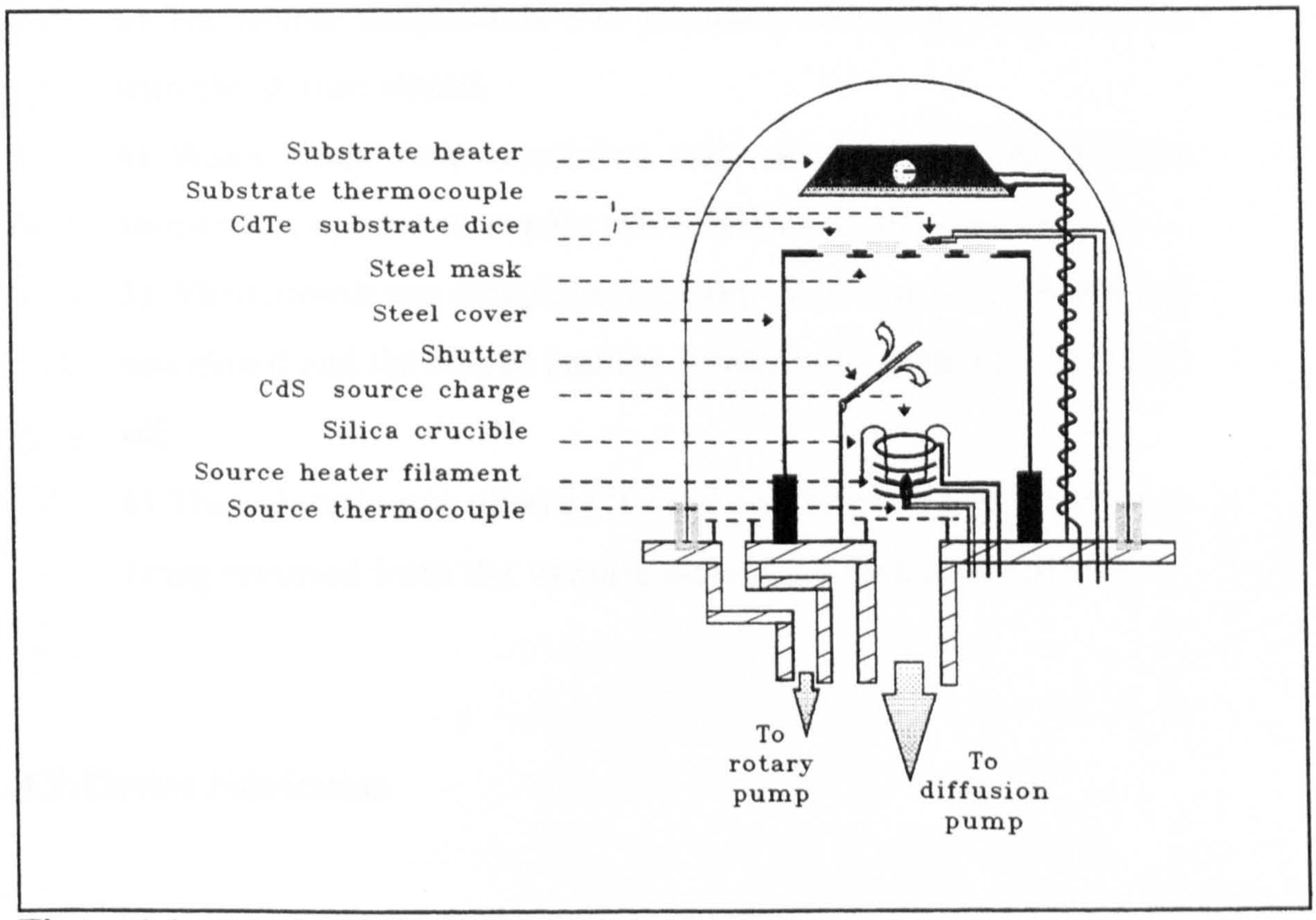

Figure 4.6 .. Schematic diagram of the bell jar fittings of the evaporator used in the deposition of CdS.

was inserted into the crucible. A stainless steel shutter operating via a rotary knob, positioned immediately above the crucible was used to mask the substrates from the source during outgassing and start-up procedures (i.e. until the evaporation rate had attained the desired steady value).

Typically about 1 gram of CdS powder, was loaded into the crucible for each evaporation. It was covered with a thin layer of quartz wool to prevent spattering of the charge onto the substrate. The full evaporation cycle was as follows:

1) The polished p-CdTe substrates were mounted into a stainless steel mask and placed on the substrate holder in the vacuum system.

2) The system was evacuated to a pressure less than 10^{-6} mbar, and the substrates were heated to 180-230°C.

3) The source temperature was gradually increased to 700-800°C with the shutter closed.

4) When ready state conditions were attained, the mechanical shutter was opened to expose the substrate to the CdS vapour.

5) When growth was complete (typically 10-20 minutes) the shutter was closed and the source and the substrate heating were switched off.

6) The substrate was allowed to cool to room temperature before being removed from the vacuum system for further processing.

4.7. Device Fabrication

4.7.1. Preparation of Ohmic Contacts to p-CdTe

A variety of materials were used with CdTe:P in an investigation of how to obtain ohmic contacts. Materials studied included Sb, Cu, Au, P, and Graphite. The procedure for fabricating the ohmic back contact, which preceded the CdS deposition was as follows;

1) a thin layer of the contact material was deposited on a pad polished surface of the dice.

2) the dice was then subjected to heat treatment (200-300°C) in nitrogen atmosphere to diffuse in the material and create a p^+ skin at the back surface.

3) Finally, gold was deposited on the p^+ skin.

This sequence was done after the heterojunction had been formed for all investigated materials except graphite, where it was performed after junction formation. Further details are sited in section 8.3 of chapter eight.

4.7.2. Fabrication of CdS/CdTe Solar Cells on Bulk Crystal CdTe

The phosphorus doped substrates were polished (as in section 4.4) and contacted as described above in section 4.7.1. A fast etch in a solution of 1% bromine in methanol was performed to reveal a fresh surface of the CdTe at the face where the junction was to be created. Substrates were then loaded into the CdS evaporated system, and a thin layer (~1 μm) of CdS deposited as outlined in section 4.6. The final stage in the fabrication process was to make contacts to the CdS. Indium was used for this, while a final gold metallic layer was deposited on the back surface of the CdTe:P where a p^+ layer had been created. For the top contact, an ultra thin indium layer was evaporated first onto the undoped CdS, followed by a small and thick indium contact, where the former serves as charge collector and the later serves as the top contact to the solar cell.

After deposition of the CdS the cell was coated (on both large area surfaces) with lacomit varnish. The sample was then immersed in HCl to remove any CdS or indium that may have been deposited on the sides of the device to prevent shunt leakage currents. Devices were then mounted on copper plates which had been etched in dilute HCl, washed in deionised water, and dried in a stream of nitrogen. After the lacomit was removed from the device sides, the dice was mounted using silver paste onto the copper plate. At this stage the device became ready for characterisation.

4.7.3. Preparation of Schottky Barrier Devices

Schottky diodes were used for characterisation of the material and optimisation of the ohmic contacts to p-CdTe. High resistivity CdTe crystals grown in this laboratory (section 4.3) were first cut into 5 × 5 × 1.8 mm^3 dice using a diamond saw. After cleaning in acetone the dice were polished mechanically and chemically as outlined in section 4.4. The dice were then doped p-type as required using the procedures described in section 4.5 and then polished

again to remove any surface layer of excess tellurium. This was followed by a pad polish in 2% Br-methanol solution for 3 minutes.

Indium was used to make the rectifying contact and other materials were applied to form ohmic contacts as outlined in section 4.7.1. After polishing, the doped dice were mounted onto a stainless steel mask with holes of different diameters and loaded into an oil-pumped vacuum system capable of providing vacuums in range of 10^{-4} mbar. Indium was then deposited by evaporation from a molybdenum boat. In order to avoid scratches and oxidization of the In layers they were left in the system for a couple of hours after evaporation was completed and were then covered with thin layers of silver paste.

Characterisation tools are introduced in the following chapter. The optimisation study of the PGD process is discussed in chapter 6 together with the structural and electrical properties of the resulting semiconductor. Device performance and analysis follow in chapters 7 - 9.

4.7. References

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Chapter V

Characterisation Techniques

5.1. Preface

This chapter focuses on the experimental techniques used in the assessment of the materials and devices investigated. Characterisation techniques are classified according to their application in the current study. For example, the transmission electron microscope (TEM) and the scanning electron microscope (SEM) (with its SE, EDX, & CL modes) techniques are described in the structural characterisation section (5.2), while the I-V, C-V, SR, and the EBIC mode of the SEM are contained in the device characterisation section (5.4). A third section (5.3) on the electrical characterisation of the materials, includes resistivity and Hall coefficient measurements. These experiments are all well established and the reader is referred, for more details, to relevant textbooks and review articles whenever appropriate.

An intensive section on solar simulators is also included in this chapter. It starts with a literature review and ends by introducing an updated solar simulator.

5.2. Structural Characterisation..

The introduction of impurities into a semiconductor results in a disturbance of the surface and the bulk lattice. In order to optimise the PGD treatment therefore it was necessary to monitor possible changes in the morphology of the material. For this purpose, both scanning and transmission electron microscopies were used. The SEM was used in the SE, EDX, and CL modes, descriptions of which follow in sections (5.2.1.1-3). The SEM in the EBIC mode was also used in the electrical assessment of the fabricated devices. A

description of this mode is given in the electrical characterisation section (5.3). The author wish to thank Dr. Y.Y.Loginov for his work on the TEM measurements and C.C.R.Watson for his work on the CL assessment.

5.2.1. Scanning Electron Microscopy (SEM)..

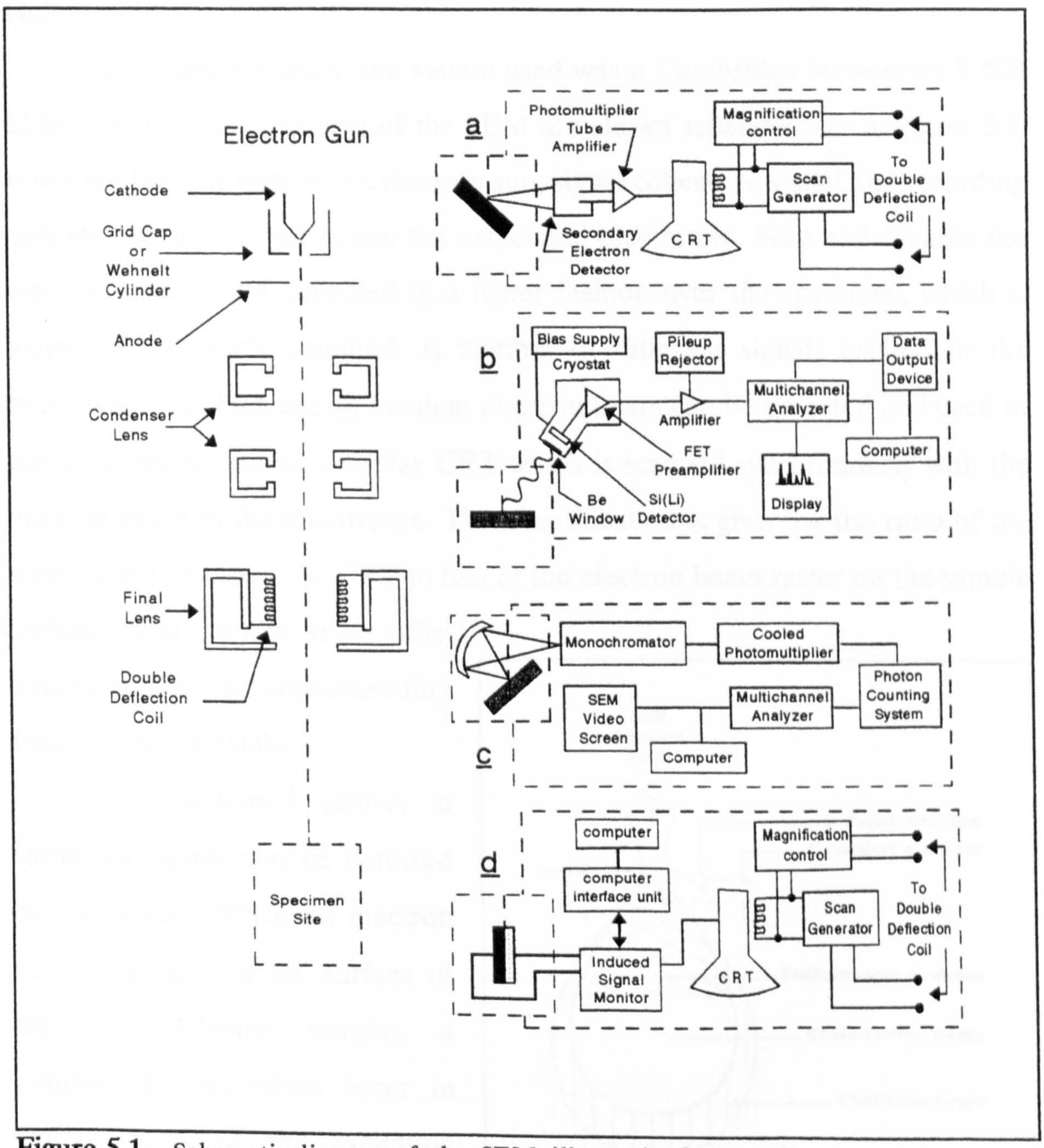

Figure 5.1 .. Schematic diagram of the SEM illustratingfour applicationsof the system, for a; SE, b; EDX, c; CL, d; EBIC modes.

Scanning electron microscopy (SEM) techniques are well suited for the microcharacterisation of semiconductors, since they provide high spatial resolution and the simultaneous availability of a variety of modes and forms of contrast [1]. The construction, modes of operation, and uses of the scanning electron microscope are described in detail in the textbooks by Goldstein et al [2,3] and Holt et al [4].

In the present study, the system used was a Cambridge Stereoscan S 600 SEM. The basic components of the SEM are shown schematically in figure 5.1, which are the lens systems, an electron gun, signal collectors, visual and recording cathode ray tubes (CRT's) and the associated electronics. Scan coils enable the electron beam to be deflected in a raster fashion over the specimen, which is maintained at earth potential. A number of different signals excited in the specimen by the high energy incident electron beam can be detected and used to modulate the output of a display CRT which is scanned synchronously with the electron beam in the microscope. The magnification is given by the ratio of the width of the image on the CRT to that of the electron beam raster on the sample surface. Most modern SEMs offer a range of magnifications extending from ×20 to ×100,000.

As mentioned above, a variety of signals may be detected by the system. When an electron beam impinges on the surface of the semiconductor sample, a number of interactions occur in various parts of the excitation region within the sample, as illustrated in figure 5.2. In

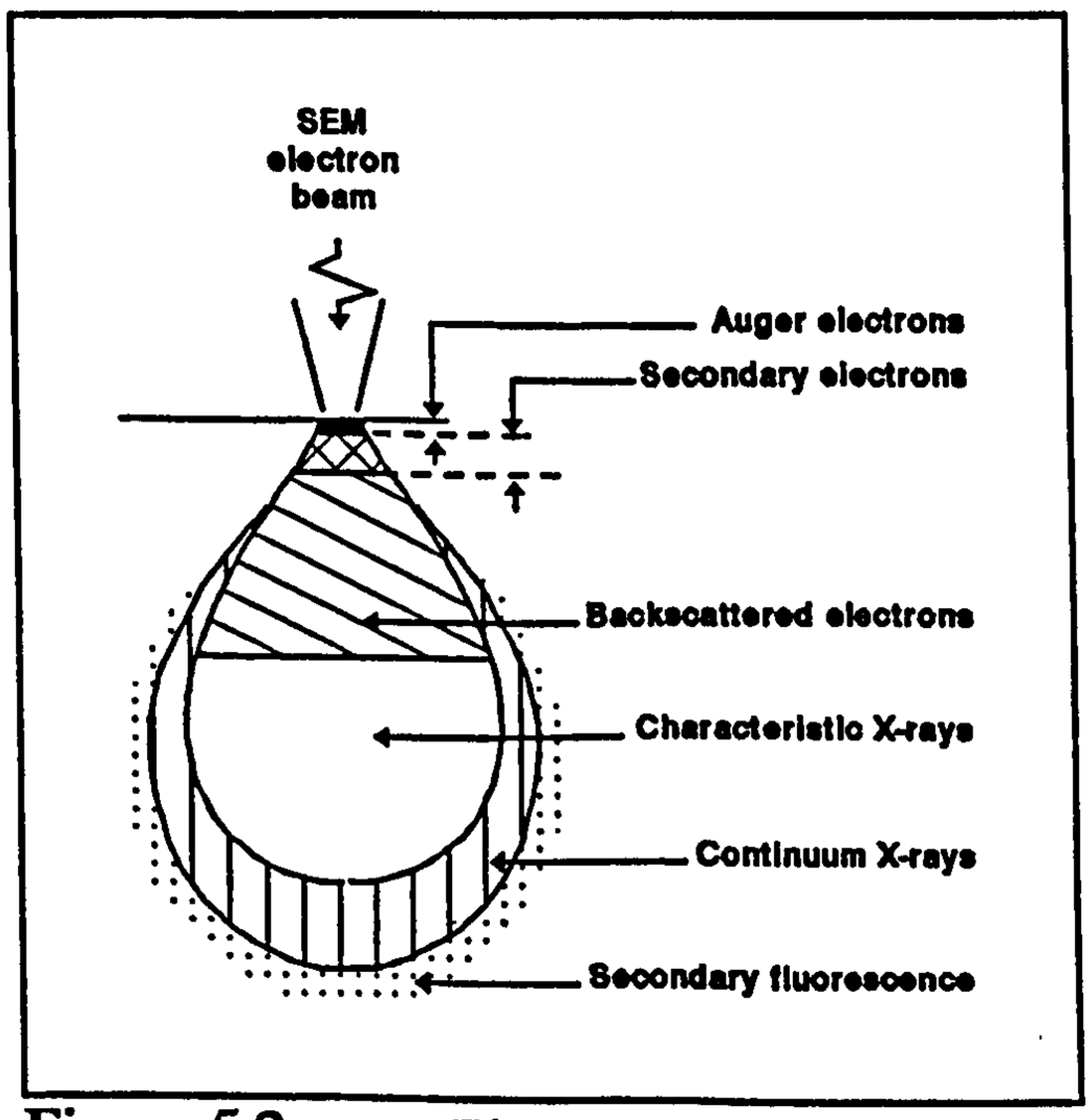

Figure 5.2 .. Electron beam-specimen interactions.

particular, the incident electron beam will generate:

(i) secondary electrons which may be collected to form a magnified image of the specimen surface. This is the secondary emission (SE) mode of the SEM.

(ii) X-rays from the interaction with atoms up to a depth of a few μm beneath the surface. These may be collected as well and analysed to give information on the elemental species present in the sample. This is the mode of energy dispersive analysis of X-rays (EDX).

(iii) electron-hole pairs within the sample. These may be extracted and displayed to give information about electrically active structural features (e.g. grain boundaries and the precipitation of impurities) and important electrical (material) parameters such as the minority carrier diffusion length. Charge generation and recombination effects can be exploited in the SEM in;

a) the cathodoluminescence (CL) mode, which constitutes the optoelectronic microcharacterisation capability of the SEM. It offers a contactless and relatively non-destructive method with high spatial resolution for microcharacterisation of luminescent materials.

b) the electron beam-induced current (EBIC) mode, which may also be used in the formation of images and signals when the generation volume intersects, or is within the diffusion length of, a potential barrier such as a p-n junction or a Schottky diode.

Three of these different modes, that were used in structural characterisation of the materials and devices, for the present work are described briefly in the following sub-sections. The fourth is described in section (5.3) together with the electrical characterisation methods Nevertheless, the four modes are all illustrated

schematically in figure 5.1(a,b,c and d).

5.2.1.1. The Secondary Emission (SE) Mode

In the SE mode of operation the secondary electrons emitted from the sample are collected and imaged. The number of electrons emitted is a function primarily of the surface topography and of the variation of secondary emission efficiency across the surface. The secondary electrons are collected by an Everhart-Thornley detector. This consists of scintillator and Faraday cage arrangement coupled to a photomultiplier tube. The secondary electrons are too low in energy to excite scintillations and so these low energy electrons are accelerated by applying a potential of +14 kV to the scintillator. To screen the primary electron beam from the influence of the high potential, the scintillator is surrounded by a Faraday cage biased at +250 V to collect the primary back-reflected and secondary electrons. The collected electrons are then accelerated onto the scintillator producing flashes of light (scintillations) which are transported via a light pipe to the cathode of the photomultiplier to initiate a cascade of electrons. In this way a very large gain with very little noise is obtained. The photomultiplier signal is applied to the z-modulation of a CRT display which is scanned in synchronism with the primary electron beam to give a video image of the surface. By confining the area of the sample scanned, and using a well-focussed beam it is possible to obtain very high levels of magnification with good depth of field. This mode of the SEM was successfully used to study the morphology and cross-section of the materials.

5.2.1.2. Energy Dispersive Analysis by X-rays (EDX)

For the EDX mode, the SEM was linked with a system 860 analyser. Analysis of the X-rays enables the chemical composition of the area under study to be determined [5]. This is an invaluable facility for the identification of the

elemental composition within a selected region of the surface on which the stationary electron beam is positioned. In this mode of operation the characteristic X-rays are produced by electron bombardment provided the accelerating voltage is greater than the critical potential. Characteristic X-rays are emitted due to electronic transitions between sharp, inner-core levels. The lines, therefore, are narrow, characteristic of the particular chemical element and are unaffected by the environment of the atom in the lattice. A limitation of this technique is that it can only be used to detect elements of the periodic table with an atomic number greater than eleven. However, it is useful in discerning the elemental distribution to the CdTe dice surface before and after being PGD treated, and establishing the position of the interface of a heterojunction to an accuracy of ~1 μm, which is the order of the width of the beam-induced excitation region.

The X-ray signal from the sample passes through a Be window into a cooled reversed-biased p-n Si(Li) detector. This leads to the formation of electron-hole pairs which are swept away by the voltage bias to form a charge pulse which is then converted to a voltage pulse by a charge sensitive amplifier. The detector works on the principle that the voltage pulse produced is proportional to the energy of the incident X-ray photon. The signal is further amplified and passed on to a multi-channel analyser (MCA) where the pulses are sorted by voltage and stored. The contents of the MCA's memory may then be passed on to a computer for peak identification, by comparison with the known positions of the characteristic X-ray lines of all elements, and are then displayed on a monitor. The relative intensities of the emission lines can be measured directly from the print out spectrum, taking care to subtract the back-ground levels from the peak.

5.2.1.3. The Cathodoluminescence (CL) mode

Cathodoluminescence (CL), i.e. the emission of light as a result of electron ("cathode ray") bombardment, offers a contactless and relatively 'non-destructive' method with high spatial resolution for microcharacterisation of luminescent materials. The CL signal is formed by detecting photons of the ultraviolet, visible and near infrared regions of the spectrum. These photons are emitted as the result of electronic transitions between the conduction and valence bands and levels lying in the bandgap of the material. Many useful CL signals in these cases are due to transitions which involve impurities and a variety of defects. There is no general rule which serves to identify bands or lines in the CL spectrum [1]. CL studies offer two major advantages. Firstly, in favourable cases, i.e. when an impurity is an efficient recombination centre (which is the case for P in CdTe) and competing centres and self-absorption are absent, the detection limit can be as low as 10^{15} atoms/cm^3. This is about six orders of magnitude lower than that in the X-ray mode. Secondly, in light-emitting optoelectronic materials and devices, it is the luminescence emission properties themselves that are of practical importance. CL analysis can also provide depth-resolved information by varying the incident electron beam energy.

The essential requirements for CL detection system designs are a high efficiency of light collection, transmission and detection. Recent designs utilize a semi-ellipsoidal mirror for CL collection and a fibre-optic guide for signal transmission to the entrance slit of a monochromator. Light with a narrow range of wavelengths then falls on the photomultiplier, the output of which is a train of pulses corresponding to the incident photons. The output of the photon counter, which provides noise rejection and amplification, can then be fed through a video amplifier to a cathode-ray-oscilloscope display to produce CL images, or alternatively, subjected to computer analysis.

5.2.2. Transmission Electron Microscopy

Detailed descriptions of the construction and operation of transmission electron microscopes (TEM's) may be found in the textbooks by Hirsch et al [8] and Loretto and Smallman [9]. However, basically, a TEM consists of an electron gun, condenser (electromagnetic), objective and projection lenses with various apertures. In operation, when the parallel beam leaving the condenser lens illuminates an ultra thin crystalline sample, part of the beam will be diffracted. Whether selecting the undiffracted or diffracted electrons passing through the objective lens a pattern may be formed. Operational modes are then called bright field or dark field imaging respectively. Other modes of operation are; selected area diffraction (SAD) and scanning transmission electron microscopy (STEM). Here the latter employs an electron beam of much smaller diameter than the conventional TEM (˜0.01 μm as compared to 10 μm)and the beam is scanned across the sample in a raster fashion. In the current study a JEOL 100CX TEM was used. This facilitates both STEM and EDX modes.

5.3. Electrical Characterisation

5.3.1. Measurement of Resistivity and Hall Coefficient

The resistivity and Hall coefficient of the CdTe dice were measured using the van der Pauw method [7]. By using four ohmic contacts (arbitrarily labelled A,B,C and D), the method can be applied to flat samples of arbitrary shape. Therefore, the effect of the exact shape of the dice on the measured result is minimised so long as the assumptions on which the calculation is based are maintained. These include; uniform thickness of the sample and small contacts positioned anywhere near the periphery of the sample.

Experimentally, four gold contacts were applied to the CdTe substrates

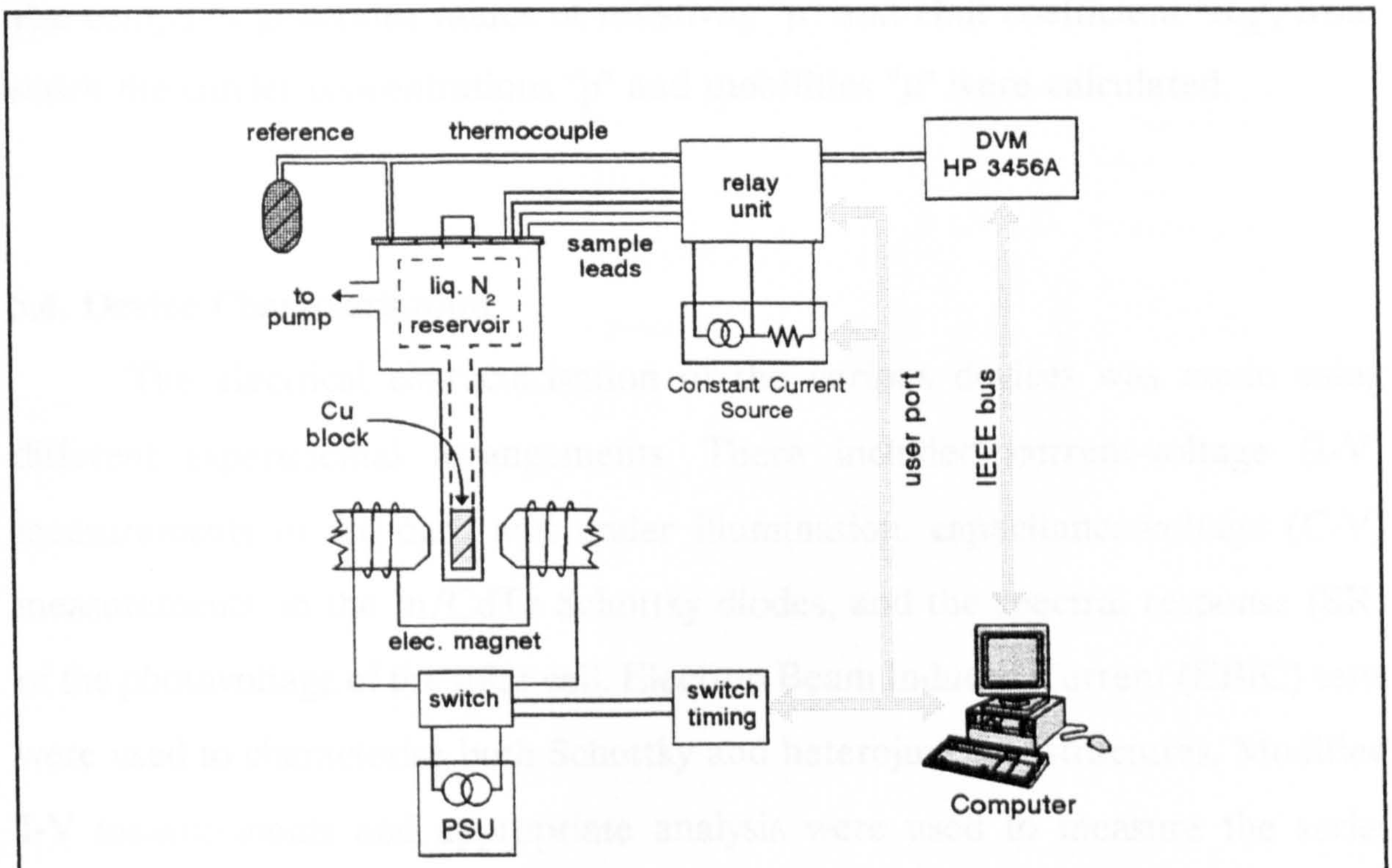

Figure 5.3 .. An outline of the apparatus used in resistivity and Hall coefficient measurements.

after mechanical and chemical polishing described in section (4.4). Measurements were made of the resistance between consecutive pairs of contacts ($R_{AB,CD}$, $R_{BC,DA}$, $R_{CD,AB}$, and $R_{DA,BC}$, where the first and second pair of subscripts refer to current and voltage terminals respectively) to provide the basis of the calculation, full details of which can be found in reference [7]. Routine determination of the Hall coefficient and resistivity over the temperature range from close to that of liquid nitrogen to room ~300 °C, were made using the apparatus shown in figure 5.3. This system is run and controlled by computer. This method of determining the resistance and Hall coefficient eliminated the effects of offset potentials and provided some averaging. The measured data were readjusted using the gradient of a least square fit. The current scans were performed in both forward and reverse directions to provide further averaging. In addition, the raw current-voltage data were plotted to ensure that the contacts to the sample were ohmic.

The computer generates values of resistivity "ρ" and Hall coefficient "R_H", from which the carrier concentrations "p" and mobilities "μ" were calculated.

5.4. Device Characterisation

The electrical characterisation of the various devices was made using different experimental arrangements. There included current-voltage (I-V) measurements in the dark and under illumination, capacitance-voltage (C-V) measurements on the In/CdTe Schottky diodes, and the spectral response (SR) of the photovoltage of the solar cell. Electron Beam Induced Current (EBIC) tests were used to characterise both Schottky and heterojunction structures. Modified I-V measurements and appropriate analysis were used to measure the series resistances of the devices. In the following sub-sections all these experimental techniques are described.

5.4.1. Current-Voltage Characteristics (I-V)

Detailed point-by-point measurements of the I-V characteristics were carried out using a highly sophisticated Keithley multimeter (model A195) (which contains a high impedance voltmeter and a low impedance ammeter) with the device placed in a light-tight enclosure. The bias voltage was derived from a calibrated D.C.Supply (Time Electronics Ltd. Model 2003).

The photovoltaic output characteristics were measured under simulated AM1 illumination. AM1 illumination was provided by a specially designed and constructed solar simulator. Full details about the simulator are provided in section 5.5. Light and dark I-V measurements at room temperature (25° C) were made on the kit described in section 5.5.4. The sample was maintained at the desired temperature by balancing the heating effect of two thermo-couple controlled resistive heaters and the cooling of a water bath that is built into the

cell stage.

On the other hand, dark I-V measurements over a wide range of temperatures were performed while the cell was placed in a cryostat, a schematic diagram of which is shown in figure 5.4. Placing the cell in the cryostat allowed the temperature to be lowered to 77 K using liquid nitrogen, vacuum insulation and helium as a heat exchange gas. The cell was then slowly warmed up by thermo-couple controlled resistive heating so that several I-V measurements could be taken at any fixed temperature between 77 K and 400 K.

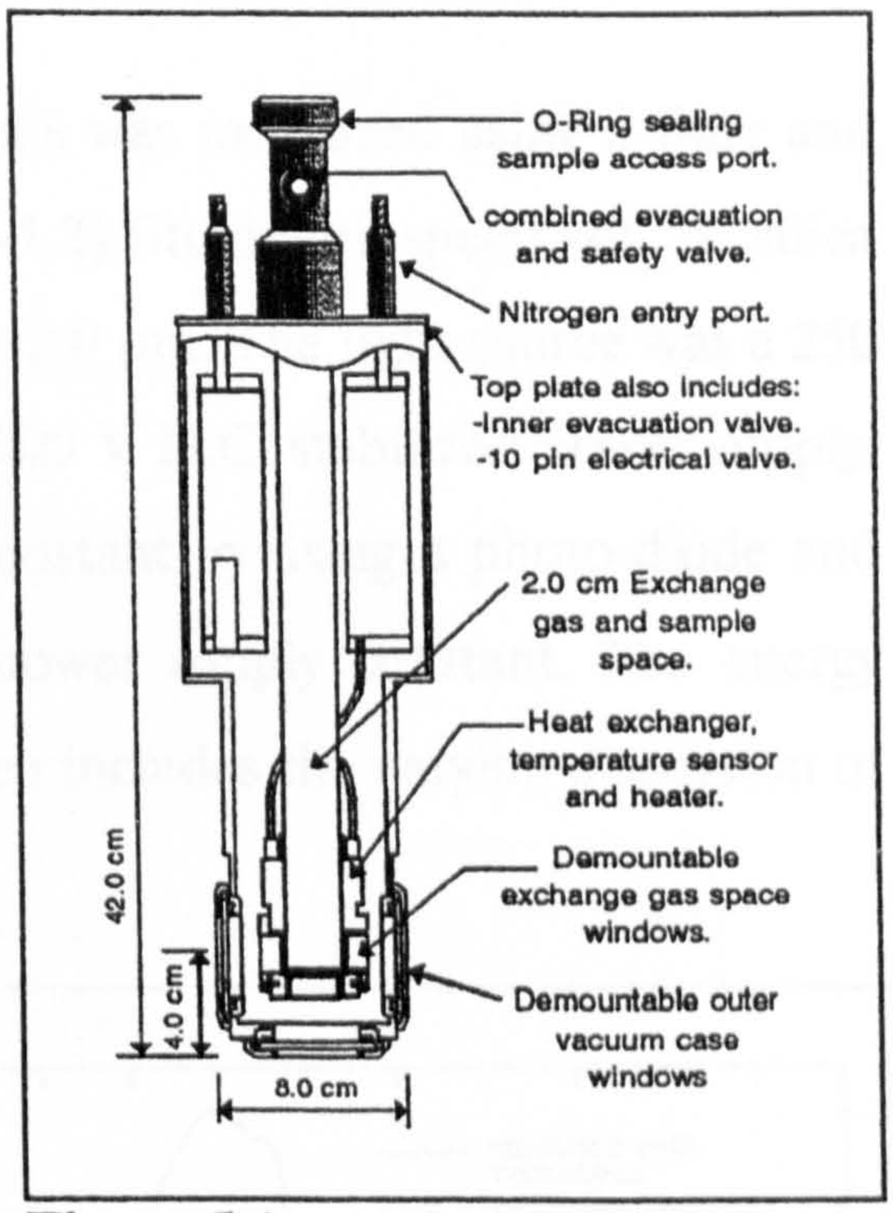

Figure 5.4 .. Liquid nitrogen cryostat (type DN 1704).

5.4.2. Capacitance-Voltage Characteristics (C-V)

Capacitance-voltage characteristics have been measured for all diode structures fabricated throughout the study, as a means of determining free carrier densities and estimating barrier widths and heights. They also give an indication of interface state activity.

Capacitance-voltage characteristics were measured manually with a Boonton 72B Capacitance meter, which operates at 1 MHz, together with a D.C. calibrated voltage source (Time Electronics Ltd. Model 2003). The sample was loaded into the cryostat shown in figure 5.4. This has facilitated C-V measurements at selected temperatures between 77 K and 400 K. Steady states were achieved by leaving the sample in the dark for a sufficient time before taking the desired readings.

5.4.3. Spectral Response Measurements

The spectral sensitivity of the solar cells was measured using a Barr and Stroud double prism monochromator (type VL2) fitted with spectrosil "A" silica prisms. The wavelength range used was 0.4 to 2.0 μm. The light source was a 250 watt, 24 volt quartz halogen lamp driven by 200 V D.C. stabilized power supply. The intensity of the light source was kept constant by using a photo-diode and lock-in amplifier to keep the illumination power supply constant. The energy distribution of the source at the exit slit, which includes the varying dispersion of the prism monochromator was measured using a thermopile with a combination of light chopper and lock-in amplifier (the light was chopped at a frequency of 10 Hz). An accurate recording of the spectral distribution of energy at the exit slit over the wavelengths $0.45 < \lambda < 0.95$ μm was made using a silicon PIN diode (type 10DF). The distributions measured with both detectors were almost identical, figure 5.5. In order to avoid the effect of drift in the monochromator the system was calibrated at regular intervals with a sodium lamp and a PIN diode. Throughout the work the width of the entrance and exit slits was adjusted to 0.5 mm.

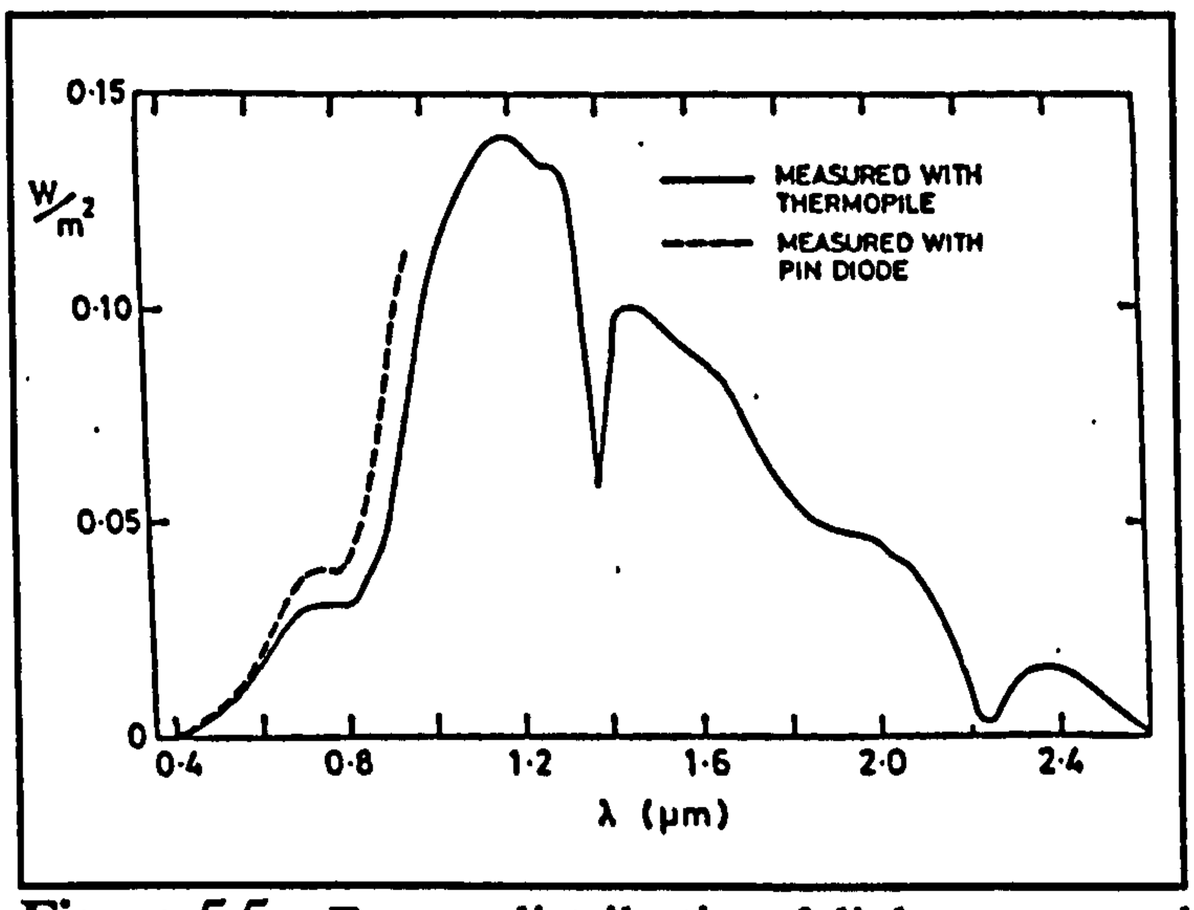

Figure 5.5 .. **Energy distributionof light source and the monochromator.**

The experimental arrangement used for photo response measurements is shown in figure 5.6. The device to be characterised was mounted on the specimen block of a cryostat and its temperature was measured with a copper-constantan thermocouple fixed to the block. The V_{oc} response of the solar cells at different

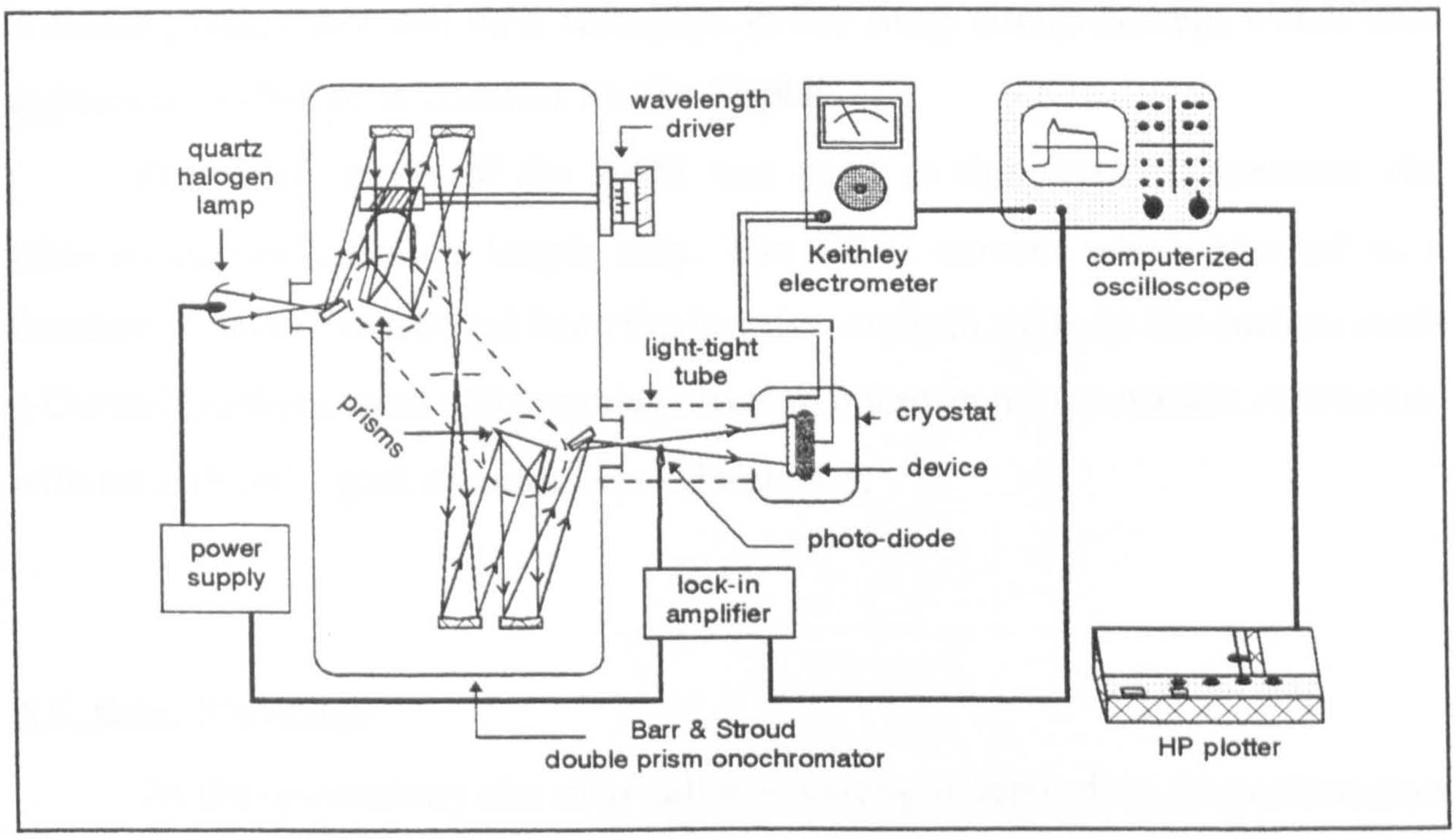

Figure 5.6 .. Experimental set up used for photoresponse measurements.

wavelengths of the incident light was measured with a Keithley 602 electrometer (of input impedance of 10^{14} ohms) directed to an HP computerised oscilloscope. The oscilloscope was used to display the input light intensity and output voltage waveforms which could then be plotted directly from the scope.

5.4.4. The Electron Beam Induced Current (EBIC) Mode of the SEM

The EBIC mode of the SEM is generally used to investigate electrically active areas in a semiconductor. This technique has been widely exploited to measure such properties of semiconductors as the minority carrier diffusion length, lifetime and surface recombination velocity [6]. A potential barrier is required, (In a Schottky or p-n junction diode) in order to separate the electrons and holes generated by the incident electron beam, in an analogous way to the photovoltaic effect. The separated charge carriers are collected, amplified and applied to the z-modulation of the CRT display. Thus, as the electron beam is scanned across the sample areas where for example preferential recombination

is taking place, there will be a reduction in the short circuit current which then appears as a change in contrast on the display.

The EBIC mode of the SEM was used in this work to measure the minority carrier diffusion length only. The EBIC current was measured as a function of beam distance (x) from the junction on both sides. In the current study a Cambridge Stereoscan 600 scanning electron microscope was used in connection with an induced signal monitor type Matelect-5.

5.5. Solar Simulator

As the responsivity of a solar cell is wavelength-dependent, its performance is significantly affected by the spectral distribution of the incident radiation, which with natural sunlight varies with location, weather, time of the year and time of the day. For example if the irradiance is measured with a thermopile-type radiometer, which is not spectrally selective, the measured conversion efficiencies can vary by as much as 15% from day to day at the same place, due to changes in the spectral distribution [10]. The solar cell performance can be obtained either by averaging over an extended measuring period, or by waiting until the actual irradiance is identical to the average. It is obvious that this is impractical for experimental line acceptance tests and for the development tests of new cells. Consequently, the sunlight has to be simulated with an artificial light source, a SUN SIMULATOR.

A solar simulator, in its simplest form, consists of a source of light, filters and a small stage. In fact many variables have to be adjusted to meet actual terrestrial conditions. Two types of solar simulator suitable for photovoltaic performance testing are usually used and commercially available, the 'steady-state' type and the 'pulsed' type. The steady state type is suitable for single cells and small modules [10,11], nevertheless, its main disadvantage is the input heat to the

test sample. The pulsed type; besides, giving uniform illumination over large areas, has the great advantage that there is negligible heat input to the test sample, but a disadvantage of the system is that each pulse of radiation measures only one point on the I-V curve [14].

In this part of the chapter, some aspects of solar simulators are reviewed, upon which an updated simulator is introduced.

5.5.1. Solar Radiation

The spectrum of sunlight extends from the ultraviolet through the visible to the far infrared as shown in figure 5.7 [ref.19]. Solar radiation just outside the earth's atmosphere is described as having an intensity of air mass 0 (AM0) corresponding to 138 mW/cm^2. The air mass 1 (AM1) spectrum represents sunlight at the earth's surface for optimum earth conditions with the sun at the zenith, leading to radiation with an intensity of about 100 mW/cm^2. The air mass 2 (AM2) spectrum in figure 5.7 represents the sunlight received at the earth's surface when the sun is at an angle of 60°, leading to a total incident power of 72-75 mW/cm^2. The major difference between sunlight in space and at the earth's surface is that ultraviolet light is filtered out by ozone in the upper layer of the atmosphere and

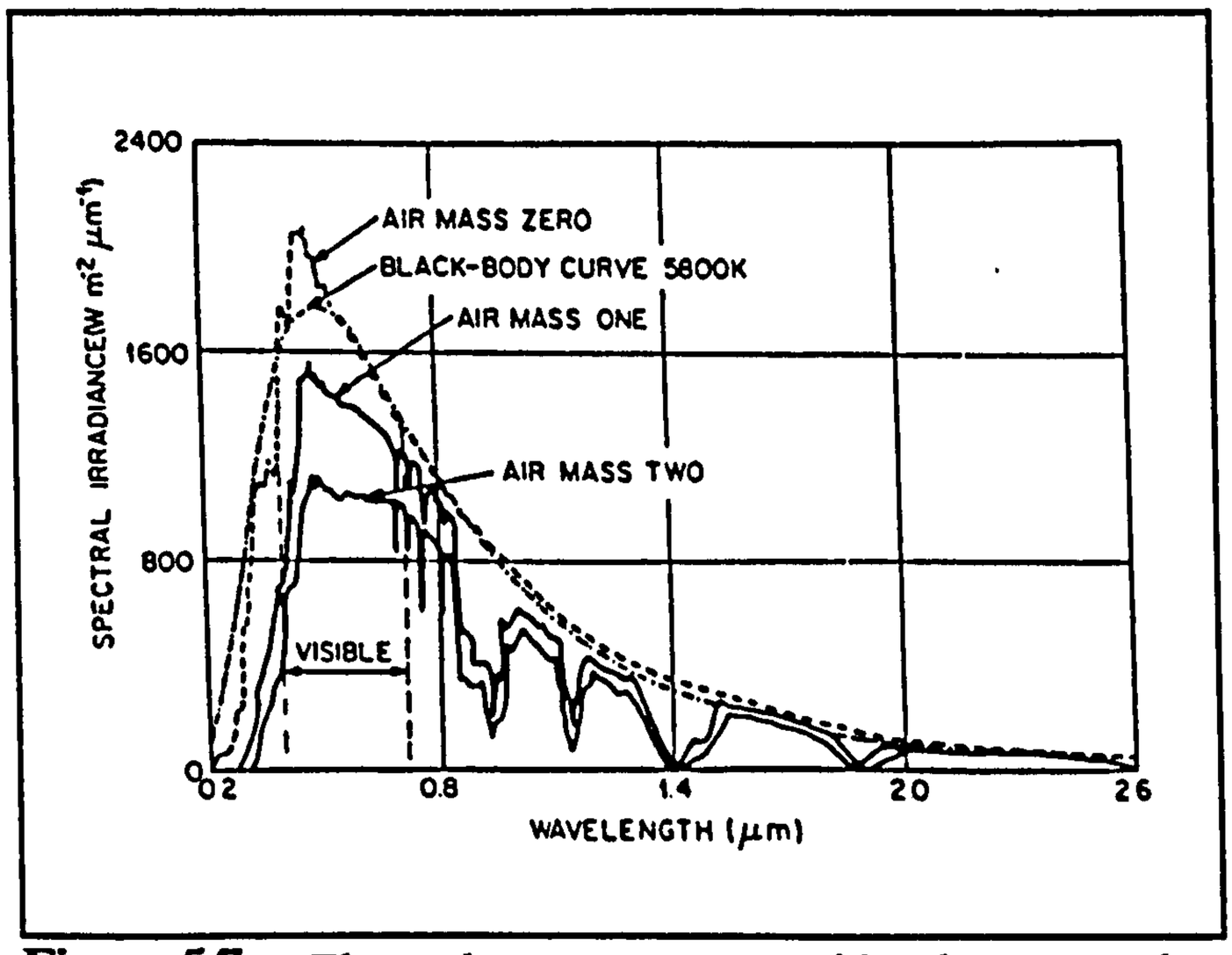

Figure 5.7 .. The solar spectrum outside the atmosphere (AM0), at sea level (AM1), and for average atmospheric conditions (AM2).

infrared is removed from spectrum by water vapour and carbon dioxide.

5.5.2. The Simulation Requirements

As the performance of a solar cell depends on the spectral distribution of the irradiance source, frequent calibration should be carried out. The best method of calibrating the simulator is to use a reference solar cell or module, that is to say a cell or module having essentially the same configuration [11,13] and relative spectral response as the test cell and module [10,11]. The short-circuit current of which in standard sun light at 1kW/m^2 has been pre-determined at a controlled temperature by an approved Solar Cell Calibration Agency.

Simulators should meet the following requirements:

Total Irradiance: The total irradiance should not be less than 1 kW/m^2, as measured with a suitable reference cell [11], 1000 W/m^2 nominal [12].

Spectral Match: The spectral irradiance (energy) distribution should match standard sunlight to the extent necessary to limit to less than ±1% error in the short-circuit current errors due to the maximum possible response mismatch between the reference cell and the test cell [10,11].

Uniformity: The uniformity should be better than ±2% as measured by a solar cell detector for less than 1/4 of the test cell area [10,11].

Total Stability: For the case of steady state-simulator, the irradiance as measured by a solar cell detector less than quarter of the test cell area, should not fluctuate by more than ±1% during a performance measurement [10,11], while a ±2% fluctuation is also accepted [13].

Beam Subtended Angle: The angle subtended by the

apparent source of the simulator on a point on the test cell must be less than 30° [10,11].

Further details about the requirements of solar simulation may be found in references [10-13]. Simulators should be checked at regular intervals and whenever a lamp, filter or optical component is changed, to ensure that the above requirements continue to be met.

5.5.3. Measurements in Simulated Sunlight

Several papers and reports [10,11,15] have been written describing performance measurement procedures for terrestrial solar cells, modules and arrays, with the aim of reducing discrepancies to an acceptable level and enabling all engaged in research, design, development, marketing and procurement to rate the performance of photovoltaic generators on an agreed common basis.

In addition to the spectral requirements, other factors need to be considered:

The temperature should be maintained at 25°C/28°C (±2°C) (the European/American photovoltaic community standards) during the performance test by mounting the cells on temperature-controlled blocks [10,11].

The measurements should be taken using four terminal contacts (current (+,-) , voltage (+,-)) [10,13,16].

If the beam is sufficiently wide and uniform, the reference cell and test cell may be mounted side by side in the same plane. Otherwise, the reference cell is replaced by the test cell, mounted at precisely the same distance from the simulator [11].

For every irradiance the current-voltage curve of the test cell may be different (18,19). An easy control of the irradiance can be used, that is to alter the bias voltage of the lamp or its distance to

the cell (19).

5.5.4. The Solar Simulator in Durham

As part of the research, the output power of the fabricated photovoltaic cells needed to be measured and compared to study various effects and correlate cell output with relevant published data. Therefore, a solar simulator was required to give fixed conditions of illumination and temperature when put under use. Therefore, a new simulator of the steady-state type has been designed and built in Durham. A general view of that simulator is given in figure 5.8. The whole of the design is isolated in a wooden container and painted on the inside with a matt black colour. The vacuum stage (shown in figure 5.9) and its components are also painted black. The distance between the tested cell and the source of light can be adjusted, and the whole system is critically leveled. AM1 illumination was provided using a 1.5 kW quartz halogen strip lamp with a parabolic reflector housing. The lamp was mounted in a levelled stainless steel frame fitted with a

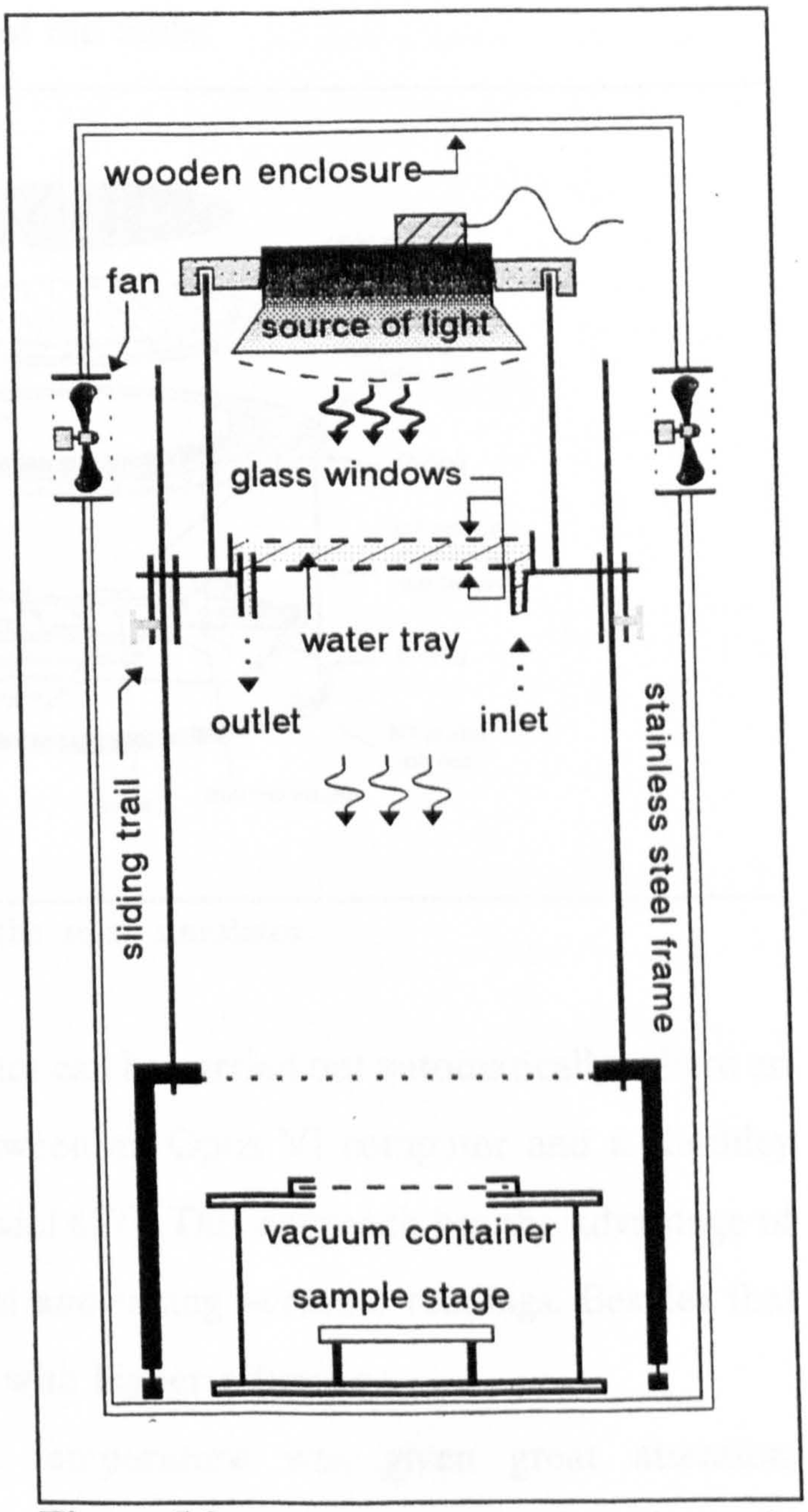

Figure 5.8 .. A general view of Durham solar simulator.

tray containing 2 cm deep flowing water intended to simulate infrared absorption of the atmosphere. The intensity of the illumination at the sample surface was measured using a calibrated silicon PIN diode and adjusted to give 1000 W/m^2 illumination by adjusting the height of the table.

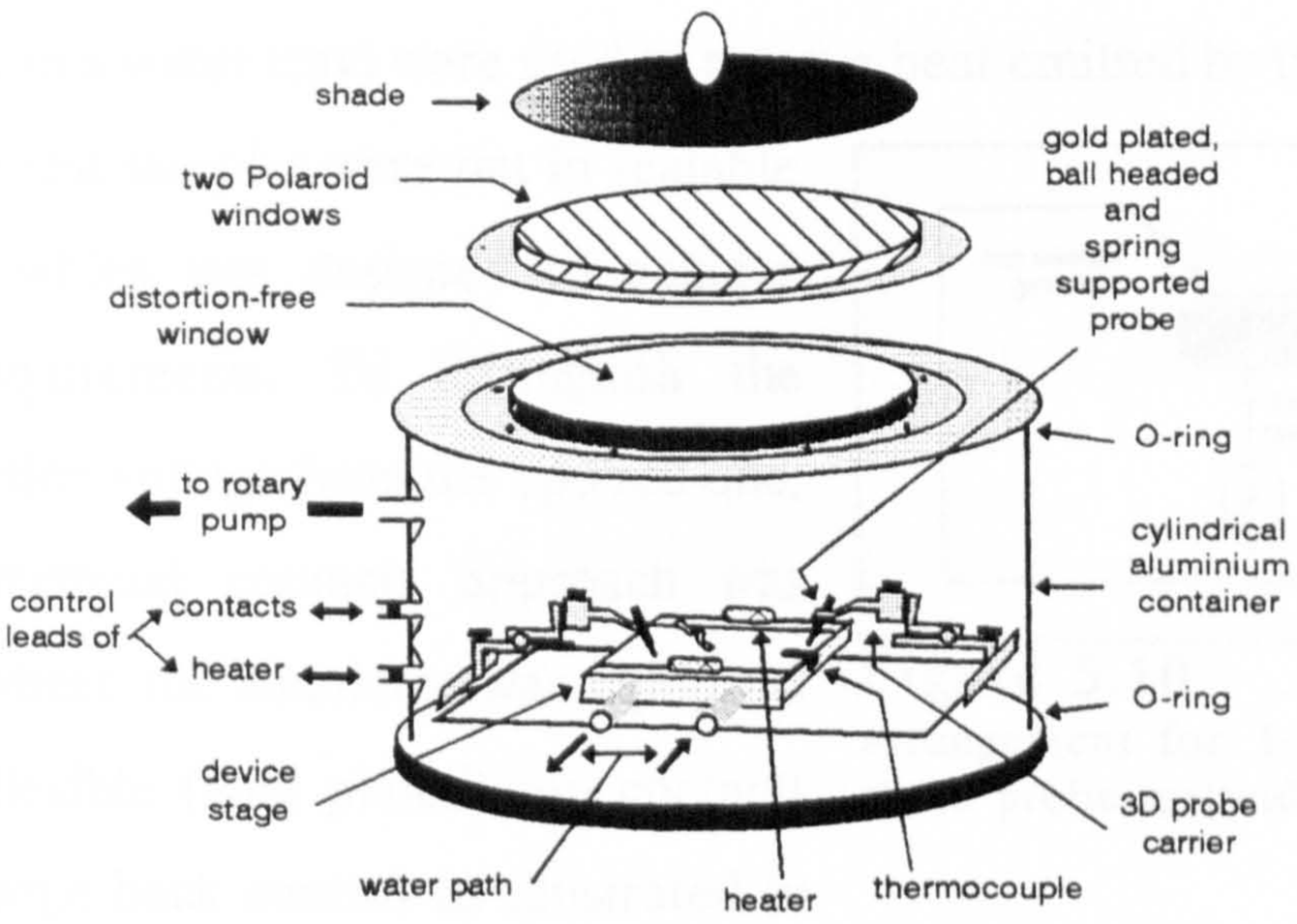

Figure 5.9 .. The device container of the solar simulator.

Measurements in this simulator can be carried out automatically, where an IEEE D-A convertor mediates between an Opus VI computer and a Keithley electrometer and power supply (model 617). This approach has the advantage of shortening the measurement period and taking accurate readings. Besides that output data is stored and analysed with higher efficiency.

The stability of the test temperature was given great attention. Thermocouples or other sensors attached to the front or back of the cell may not register the cell temperature to the required accuracy, and correction may therefore be necessary. The recommended way to alleviate these problems is to shorten the period of the test, to shade the cell from the simulator, and to maintain the cell in a vacuum container equipped with an easily cleaned

distortion-free window (11,14). All these aspects were addressed in the new simulator. It was decided to use 25°C, the European standard, as the test temperature, which was determined by the aid of two ohmic heaters driven by a temperature controller and the water bath built into the sample stage. An air current (generated by two fans) and a stream of water (sandwiched between two glass layers in a water tray) were used to remove heat emitted by the light source.

The test samples were put in sealable container, which was designed to achieve special requirements. To distinguish the actual junction voltage from the applied one, a three terminal contacts approach was adapted, where the simulator was equipped with two flexible (gold plated) top contacts and one large back contact as illustrated in figure 5.10. Another advantage of the system is that I-V characteristics could be measured under several illumination levels, since the vacuum container could be covered either with a visible distortion-free window and a pair of polaroid layers to provide any intensity between full illumination and full darkness.

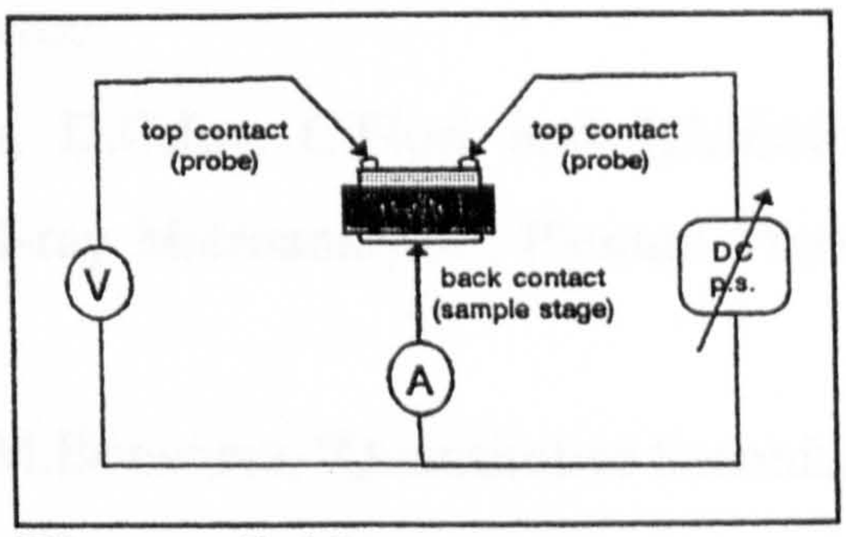

Figure 5.10 .. Experimental arrangement for I-V test using a three probe method.

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Chapter VI

CdTe:P by Post-growth Doping

6.1. Preface

For solar cells made on CdTe substrates the performance is often limited by the high resistivity of p-type CdTe which yields devices with high series resistance, and as a consequence low fill-factors and efficiencies. The most successful acceptor dopants for CdTe have been transition elements from group I, eg. Cu, and group V elements, eg. As and P, [1-5], but self-compensation [6] presents a major difficulty. Dopants are usually introduced into CdTe during crystal growth, however, this was not possible in the present study and so a post-growth doping procedure for bulk CdTe crystals using phosphorus was developed with a view to achieving low resistivity p-type material.

Although post-growth doping (PGD) is a common procedure in micro-electronic engineering, there has been no systematic research into the post-growth doping of CdTe and the process is not properly understood. This chapter is concerned with the effects of post-growth treatments on single crystal CdTe and involves a comparison between two particular doping methods. Furthermore, the resulting material properties are described and a mechanism of the phosphorus diffusion is suggested. Finally, an optimised method of post-growth doping is defined.

6.2. Post growth doping parameters

The first (and main) of the two doping procedures was an open tube method (see Chapter 4) which involved heating CdTe dice in a flow of ortho-phosphoric acid vapour (using Ar or N_2 as a carrier gas), followed by an annealing

treatment in Cd or Te vapour (obtained by heating a reservoir of the element) to diffuse in the P impurity. The second method was a closed tube process in which the CdTe samples were heated in evacuated and sealed ampoules together with the impurity source, followed by an annealing step as described previously. Both methods were successful in reducing the bulk resistivity.

It is clear that a successful post-growth doping treatment mainly consists essentially of two stages; firstly covering the sample surface with a thin layer of impurities and secondly those impurities are driven into the bulk material. The effects of varying the CdTe dice temperature and treatment time were studied in both stages of the PGD for both doping methods, while the reservoir temperature was added as a parameter in the second, annealing, stage only. A preliminary investigation was carried out to determine the best procedure for preparing dice prior to doping and to select suitable impurity source material.

6.2.1. Pre-doping sample preparation

After being cut from a bulk crystal, CdTe dice were cleaned in an acetone bath. Comparisons were then made between dice that had been; (1) chemically etched, (2) mechanically polished, then etched, and (3) heat treated at 550°C for 6 hours. The etching should remove the mechanical damage introduced by the diamond saw, while heat treatment is expected to lead to a Te rich surface. A preliminary assessment of these three factors was made using the open tube doping method, and it was then assumed that any observed trends would also apply to the other doping method. After the dice had been prepared, they were mounted in the P-doping reaction tube and heated at 550°C for 2 days, in a continuous flow of H_3PO_4 vapour. When the first stage was completed the dice were then sealed in evacuated silica ampoules. The CdTe was maintained together with a Te reservoir at 550°C, while the Te reservoir was kept at 410°C. This stage of the doping process was carried out for 7 days. Table I shows the

effect of the pre-doping treatment on dice resistivity.

Table VI.I .. Comparison of the resistivities of dice given the same P-doping procedure but different preliminary preparation.

Dice preparation routine	Resistivity
Chem. Etch. (2% Br_2 in MOH)	74 Ωcm
Mech. & Chem. Etch. (as above).	60 Ωcm
Heat Treatment (550°C for 6hrs.).	630 Ωcm

The air heated dice gave the highest resistivity, this might be due to the formation of an insulating oxide layer. The chemical and mechanical treatments gave results that were similar to each other. As a consequence, it was decided to adopt the chemical etch in 2% Br/methanol as the standard preparation, after the initial acetone bath.

6.2.2 First doping stage

6.2.2.1. Impurity source selection

Phosphorus is known to act as an acceptor in CdTe converting it to a p-type semiconductor. Both compounds and elemental sources of phosphorus were utilized as the impurity source material, including: orthophosphoric acid (H_3PO_4), phosphorus pentoxide (P_2O_5), yellow phosphorus (P_4), and a mixture of P_4 and Cd. It was more convenient to test such effects in sealed tubes. Antimony (Sb) was also investigated although preliminary trials failed to give any reduction in the resistivity and so the use of Sb as a p-type dopant was discontinued. After depositing the dopant on the surface of the dice in stage 1, dice were then annealed in a Te ambient. A thermoelectric hot probe test indicated p-type conductivity for all treated dice. The resulting Van der Pauw resistivities are

presented in table II.

Table VI.II .. Resistivities achieved using various dopant sources.

Impurity Source	P_2O_5	H_3PO_4	P_4	P_4&Cd	Sb
Resistivity (Ωcm)	3100	0.107	18800	2648	2300

Orthophosphoric acid, gave by far the best results, but one may question the contribution of oxygen in the process. By inspecting the dissociation reaction sequence of orthophosphoric acid at temperature, which proceeds as follows:

$$2\ H_3PO_4 \longrightarrow P_2O_5 + 3\ H_2O$$

$$2\ P_2O_5 \longrightarrow P_4 + 5\ O_2$$

it is probable that oxygen although present does not interfere with the doping process of the open tube method since it is gaseous and will therefore pass through the system to the exhaust. On the other hand, the oxygen has no exhaust route from sealed tubes, and so it may well become involved in the closed tube doping process. Because of its greater doping efficiency with respect to CdTe resistivity, H_3PO_4 was designated as the P impurity source for our experiments in both of the two post-growth doping methods.

6.2.2.2. Dice temperature effect

Temperature plays a major role in determining crystal growth stoichiometry, and enhancing impurity diffusion, so the temperature of the CdTe dice was the first variable to be investigated in stage 1 of the doping procedure. To fulfill such an investigation, identical dice were mounted at selected locations in the reaction tube of the open tube doping method, where temperatures were well identified. This test was repeated with the sealed tube doping method. Narrow necks were made to hold 6 dice at different levels in a single silica tube,

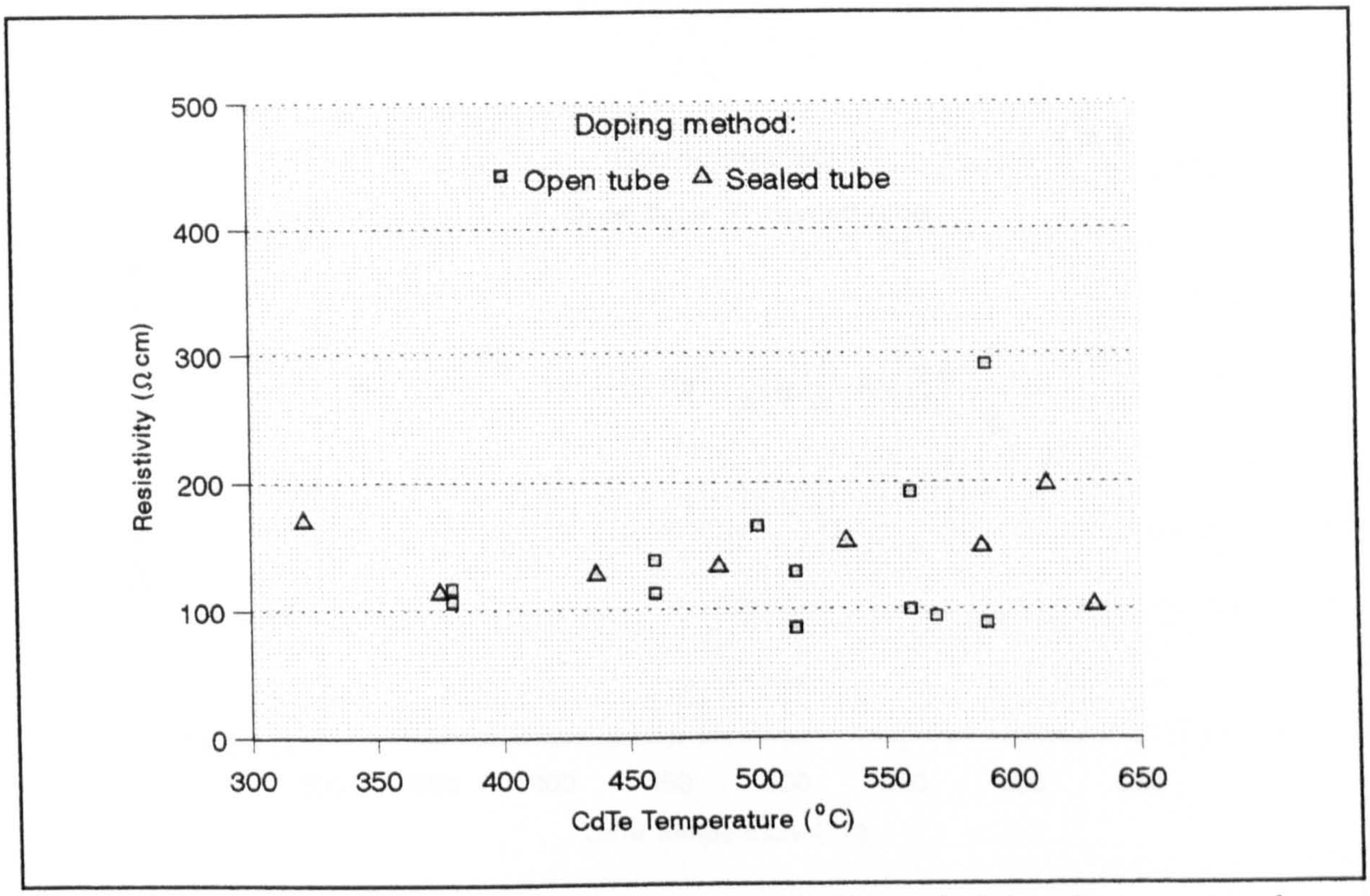


Figure 6.1 .. Stage 1 doping temperature versus CdTe resistivity. Temperature has no appreciable effect on the resistivity within the tested range in the first stage of the doping.

which was then sealed in vacuum with a little quantity of orthophosphoric acid in the bottom of the tube. This multi level tube was suspended vertically in a furnace for which the temperature gradient was known. Resulting dice were all annealed in sealed tubes by maintaining the dice at a temperature of 550°C and the Te reservoir at 410°C for 7 days.

Figures 6.1 and 6.2(a,b) show the effect of the Stage 1 doping temperature on the resistivity, carrier concentration and charge mobility of the dice, respectively. Unexpectedly, the doping temperature in the first stage of doping appears to have no appreciable effect on the CdTe resistivity, within the tested range. There was, also, very little effect on dice carrier concentration and charge carrier mobility. A similar observation was previously reported by R.B.Hall et al [7] who noted the independence of the P carrier concentration on doping temperature in CdTe.

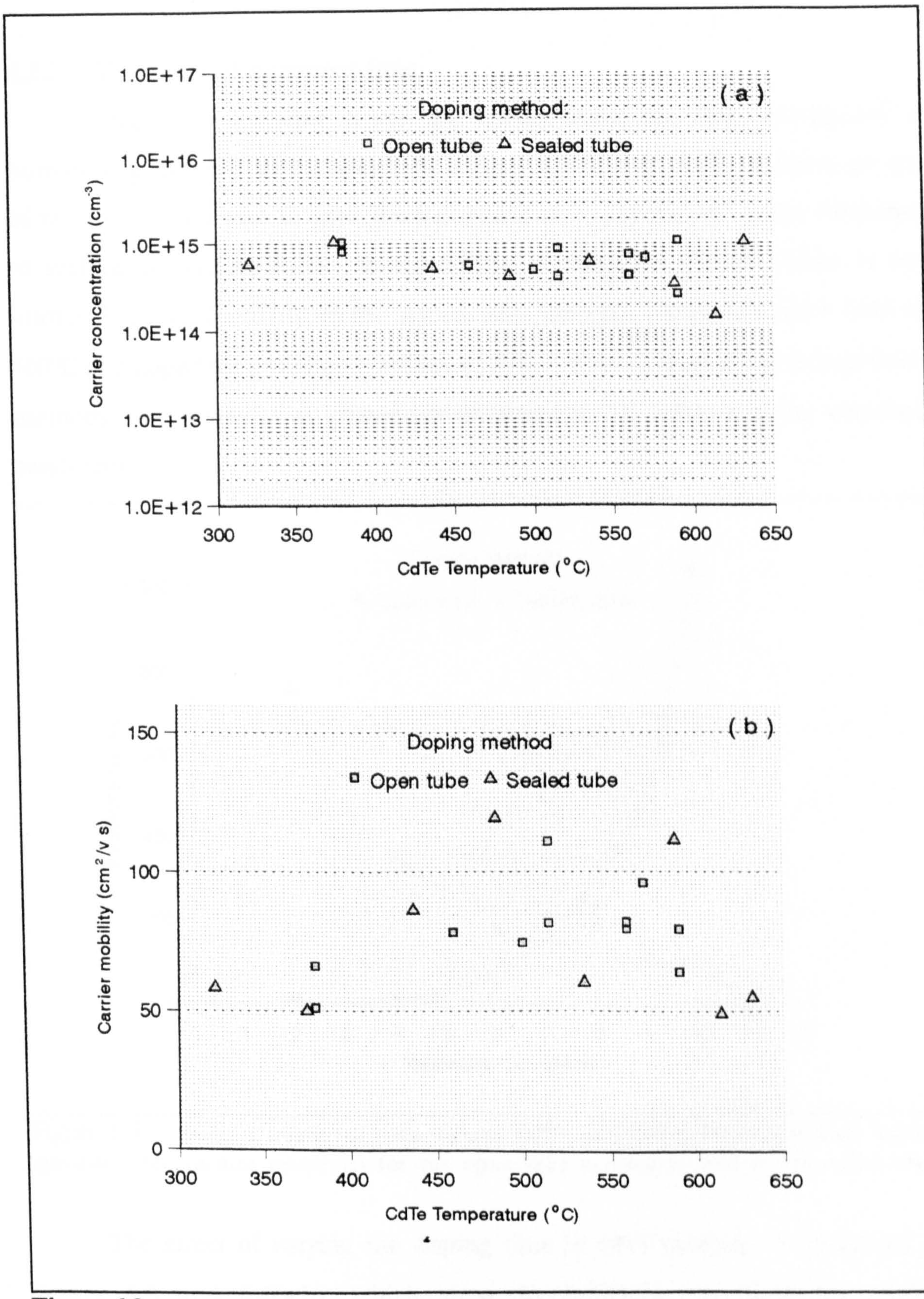


Figure 6.2 ..Stage 1 doping temperature versus (a) carrier concentration (b) carrier mobility in CdTe:P. Temp. has little effect on both p and μ within the tested range in stage 1 of the PGD.

6.2.2.3. The effect of treatment time

Time as a parameter in the first doping stage was, also, investigated in both doping methods. In the open tube method CdTe dice were treated in groups of two for 2, 4, 6, 8 and 12 days. Each doped dice in a group was either subjected to surface analysis by EDX in the SEM or electrical characteristics in the normal Hall rig. Similarly in the sealed tube method, CdTe dice were held at 400°C and doped for prolonged periods of 2, 4, 7, 8 or 11 days. All dice from both methods were annealed as previously indicated in Te ambient under standard conditions.

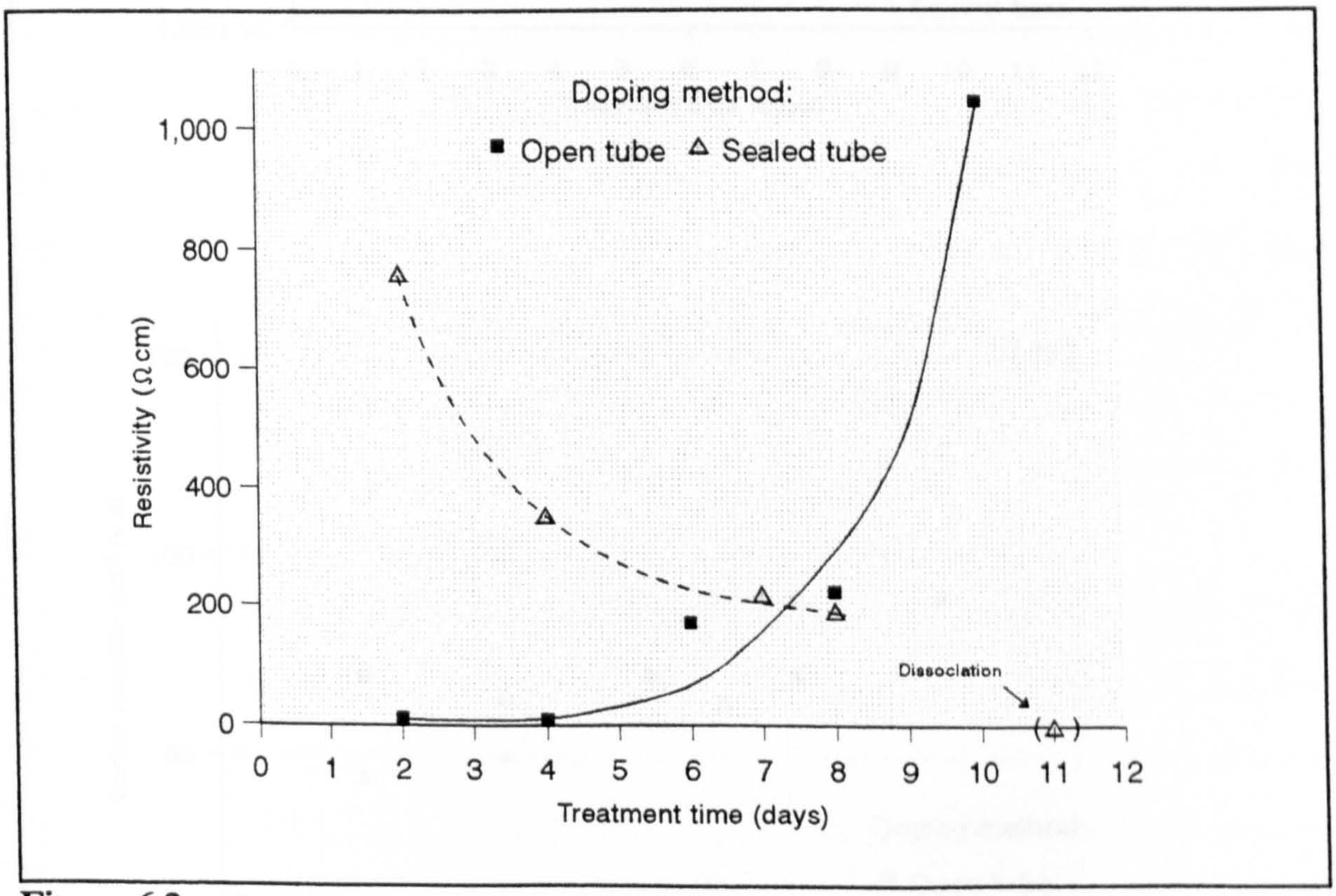
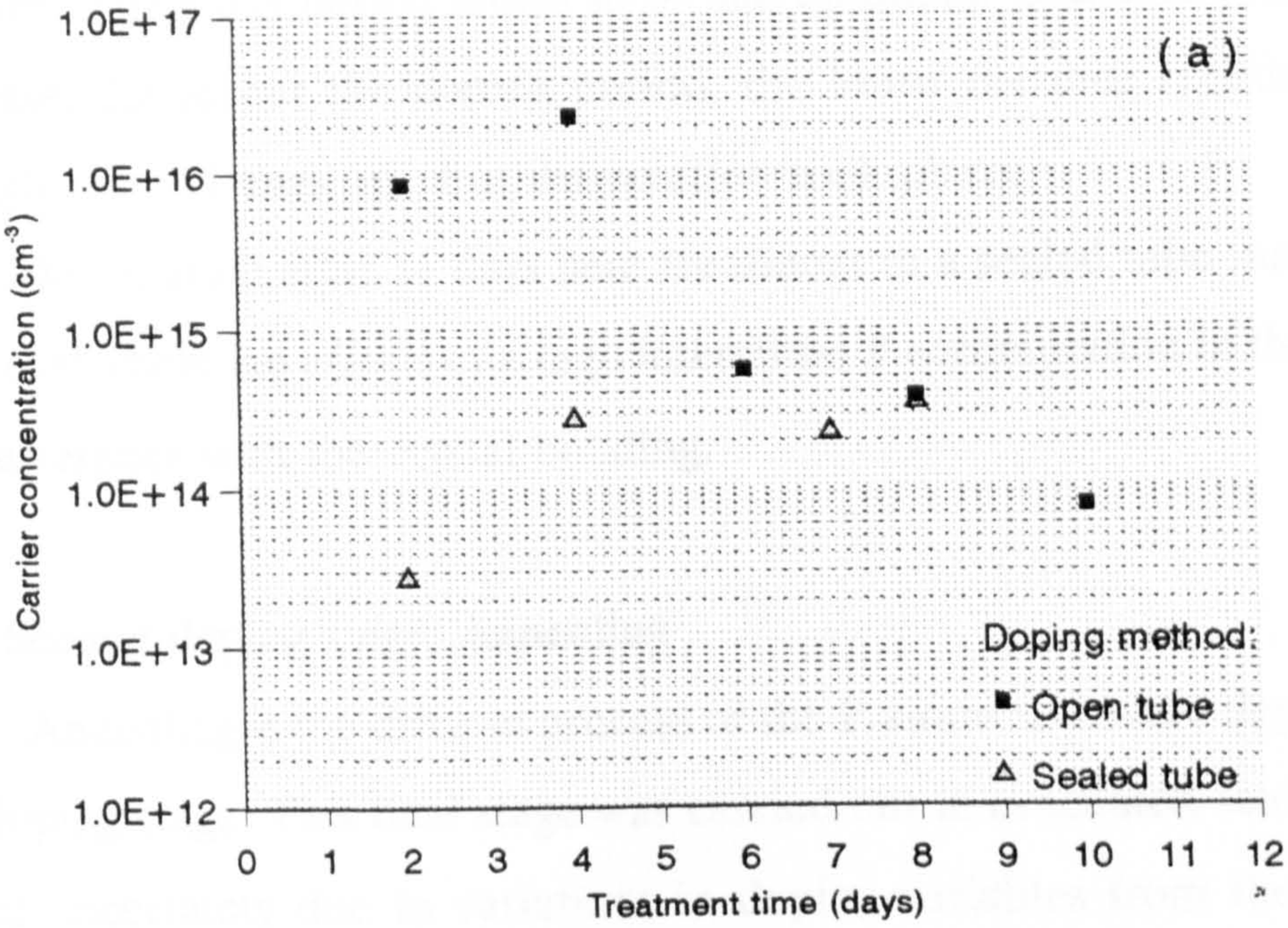


Figure 6.3 .. Stage 1 treatment time versus CdTe resistivity. Treatment time has the opposite effect on dice resistivity for the open tube method to that of the sealed one.

The effect of varying the doping time in both methods is illustrated in figures 6.3 and 6.4(a,b), which show its influence on resistivity, carrier concentration and Hall mobility, respectively. In the open tube method, 2 and 4



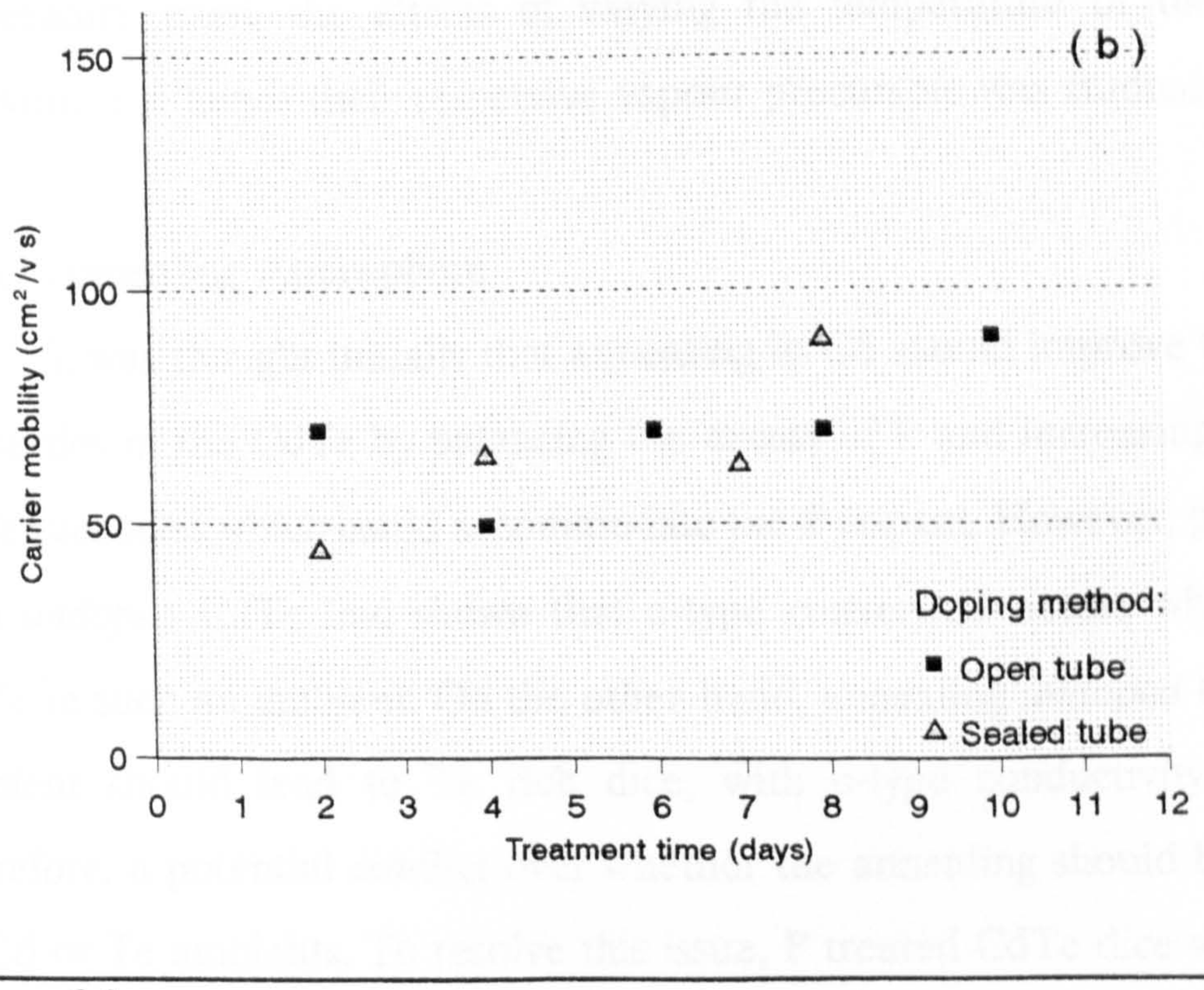


Figure 6.4 .. Stage 1 doping treatment time versus room temperature (a) carrier concentration(b) carrier mobility.Treatment time has greater influenceon p than on μ in both doping methods.

days gave excellent results, while longer periods led to a steep increase in resistivity. The 4 day period seems to be the optimum. Conversely, in the sealed tube case, the longer the doping period, the lower the dice resistivity become although after 11 days full dice dissociation took place.

Dissociation after 11 days heat treatment in a sealed tube may be related to the overwhelming effects of a high interstitial P accumulation in the lattice and its interference with the crystal bonding.

6.2.3. Second doping stage; Annealing

Annealing is the drive-in process of the P atoms that were deposited in the first doping stage. This final stage was carried out in evacuated sealed tubes. To reduce uncertainty due to variations in doping variables from the first doping stage, all the dice were obtained from a single open tube doping run. The annealing ambient was the first factor to be determined. Keeping the dice temperature fixed, the effects of varying the temperature of the Cd or Te reservoir, and hence their respective vapour precursors was studied.

6.2.3.1 Annealing Atmosphere

It was thought initially that annealing in Cd should improve the electrical properties of the CdTe by balancing the excess of P and increasing the number of Te vacancies which could accommodate the P dopant. However, previous work with *undoped* CdTe had shown that n-type conversion occurs when annealing CdTe in such an ambient. On the other hand, annealing *undoped* CdTe in a Te ambient should lead to Te rich dice, with p-type conductivity. There was, therefore, a potential conflict over whether the annealing should be carried out in Cd or Te ambients. To resolve this issue, P treated CdTe dice were annealed in Cd or Te atmospheres at different temperatures. The type and magnitude of the resulting conductivity of all dice were measured using the thermoelectric hot

probe and Van der Pauw method respectively. The samples were all coated using the 'open tube' method for 2 days. They were then annealed in evacuated ampoules together with Cd or Te and heated for 5 days at 500°C. The temperature of the Cd or Te reservoir was varied in the range of 250-600°C.

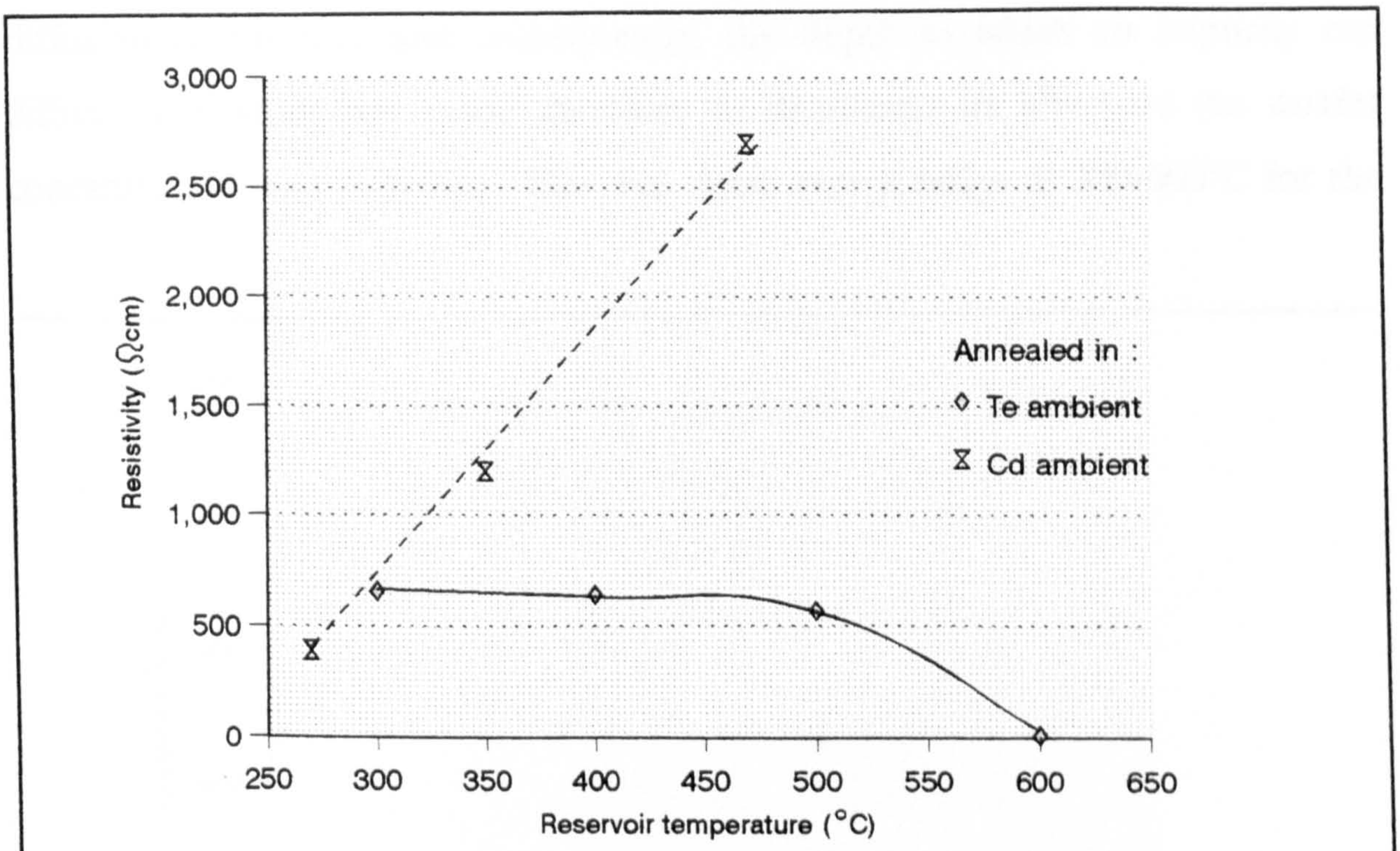


Figure 6.5 .. The influence of the annealing atmosphere at deferent temperatures on the resistivity of CdTe:P. Lower ρ could be achieved by annealing in Te rather than Cd after being treated in P.

All the dice were found to be p-type. Figure 6.5 portrays the CdTe:P resistivity after annealing in the Cd or Te ambient at selected temperatures. With the Cd atmosphere, CdTe resistivity in the tested range increased with the increase in reservoir temperature . On the other hand, when annealing identical dice in a Te atmosphere, the CdTe resistivity decreased as the Te temperature increased. Further discussion of the annealing ambient is given in section 6.3.2. It is clear that the Te/Cd temperature (in particular pressure) played an important role in controlling the resistivity and of P treated CdTe, and lower CdTe resistivities could be achieved by annealing in Te rather than Cd.

6.2.3.2 CdTe Temperature

Although the dice temperature during the deposition stage had relatively little influence on the CdTe resistivity, it was necessary to check its effect in the second drive-in stage. Fundamentally, the temperature affects the impurity diffusion coefficients, and consequently, the depth to which an impurity can diffuse-in. A study was made therefore to determine its effect on the carrier concentration, and resistivity. This was done over a range of 300-600°C for the

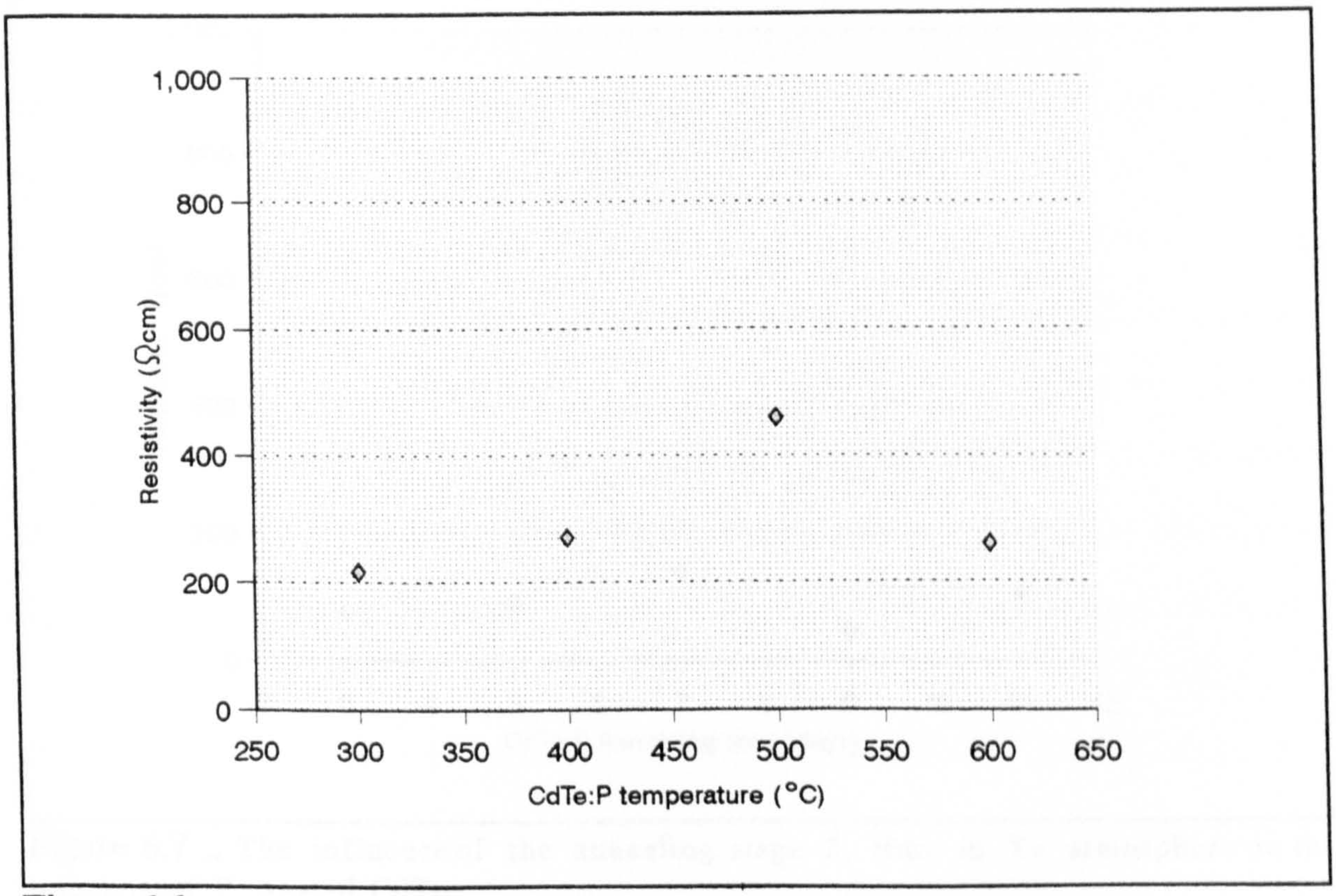


Figure 6.6 .. Resistivity versus CdTe:P "annealing" temperature in Stage 2. Dice temperature had very little influence on resistivity, carrier concentration and carrier mobility.

dice temperature, while holding the Te reservoir temperature at 400°C, for a fixed annealing time of 7 days.

Figure 6.6 illustrates the relation between the CdTe:P temperature and the dice resistivity for the above conditions. This figure suggests that the temperature had little effect on dice resistivity for the tested range. This implies that even at

the lowest temperature investigated, the annealing time of 7 days was sufficient to ensure that doping had become saturated. The lowest measurement at 300°C may be affected by the migration of Te from the Te reservoir (which was hotter in this case) to the sample. This would have a similar effect on increasing carrier concentration and decreasing bulk resistivity.

6.2.3.3. Annealing time

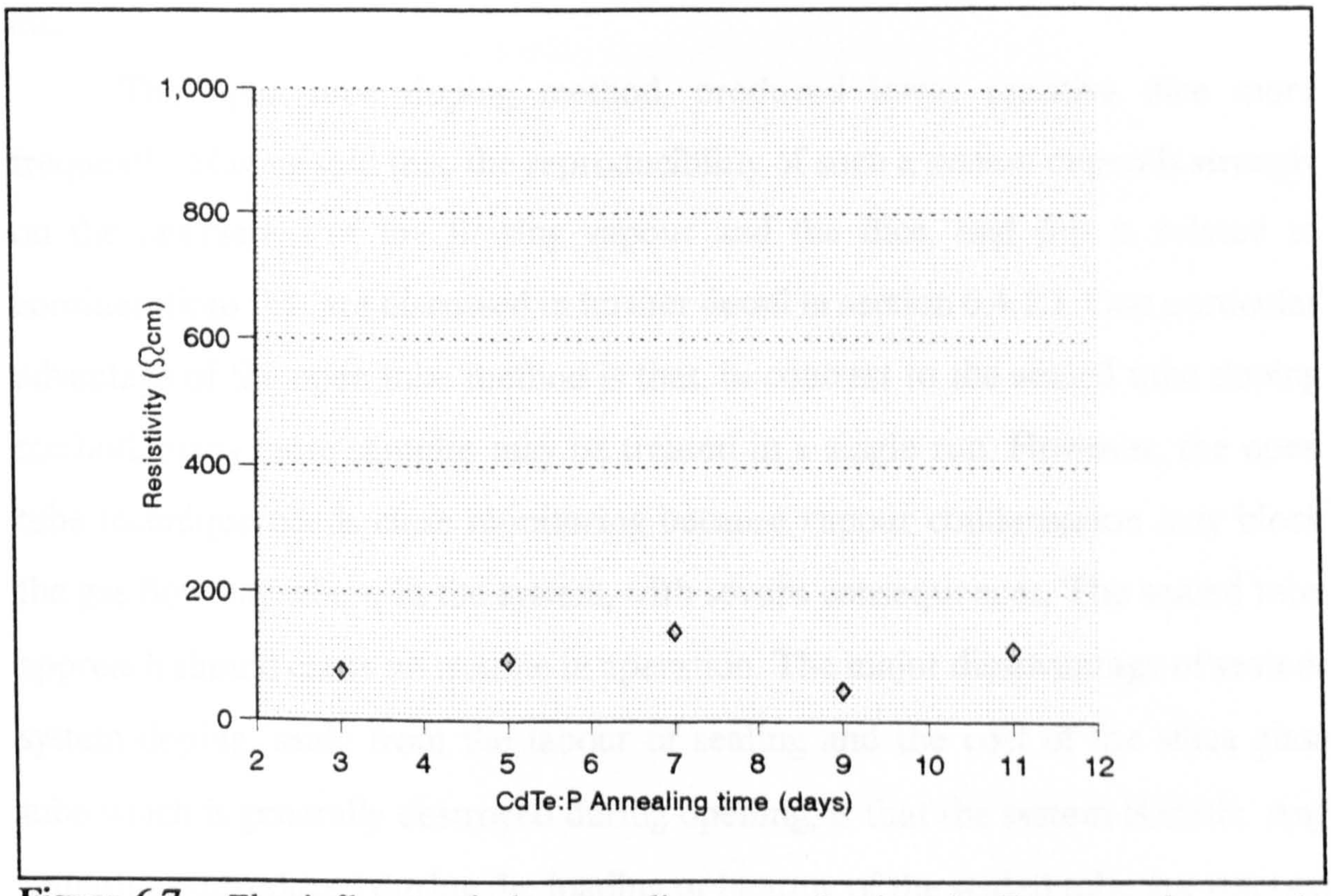


Figure 6.7 .. The influence of the annealing, stage 2, time in Te atmosphere on the resistivityof P treated CdTe.

A series of annealing trials were carried out for 3, 5, 7, 9, and 11 days, with the CdTe dice and Te reservoir temperatures held at 500 and 400°C, respectively.

The influence of the annealing time on the resistivity of the P treated CdTe is shown in figure 6.7. Surprisingly, the resistivity appears to be independent of annealing time within the range investigated, so that there was no advantage in extending an anneal beyond 3 days.

6.3. Discussion

6.3.1. Comparison between the doping methods

The experimental results from a study comparing the open and sealed tube doping methods were presented in section 6.2.2. In this section it is proposed to review these results in terms of doping efficiency, reproducibility, time involved etc.

The open tube doping method, produced lower resistive dice more frequently. Having said this, the reproducibility of such a system depends strongly on the interaction of the flowing vapour and the dice, and this is related to considerations that are discussed in further detail in section 6.4.1.1. One particular advantage of the open tube method is that, in contrast to the sealed tube doping method, many more samples may be treated in a single run. However, the open tube technique needs close monitoring because vapour condensation may block the gas flow any where in the system, with severe consequences. The sealed tube approach should cause no trouble in operation. The major disadvantage of sealed-system doping, aside from the labour of sealing and the cost of the silica glass tube which is generally destroyed during opening, is that the system is static. Any impurities introduced during the loading or heating of the sealed tube are trapped in the system and very likely become part of the diffusing impurities.

6.3.2. Annealing Role

The data from figure 6.5, can be redrawn as a graph of resistivity vs. the vapour pressure of the annealing ambient around the semiconductor in Figure 6.8. The vapour pressure of Te over the pure liquid (P_{Te}^{o}) was calculated using the empirical expression in reference [8]. Figure 6.8 shows that the resistivity of dice

annealed in a Te ambient decreased linearly with the Te partial pressure. The following empirical relationship was determined from the graph:

$$\rho = 654 - 72.4\, P_{Te}^{o} \quad (\Omega cm) \tag{6.1}$$

where P_{Te}^{o} is in mbar. Given that the resistivity $\rho \alpha 1/p$, the carrier concentration should increase monotonically with the Te vapour pressure above the dice. This may be related to the saturation of the Te vapour above the CdTe dice suppressing dissolution of the CdTe, during in-diffusion of the P.

In contrast, when the annealing is carried out in Cd vapour, the resistivity was found to increase with the vapour pressure. The Cd-anneal data of Figure 6.5 may be replotted in the same way, as a function of the Cd vapour pressure, using the following empirical expression for the equilibrium vapour pressure of Cd, P_{Cd}^{o} [8]:

$$Ln\, P_{Cd}^{o} = 26.15 - 1.8415\, Ln T - \frac{13859}{T} \tag{6.2}$$

The results of the Cd anneal are plotted in Figure 6.8b on a graph of log ρ vs. log P_{Cd}^{o} and this shows that the resistivity appears to follow an approximate power law dependence on P_{Cd}^{o}:

$$\rho = 1.4 \times 10^{7}\, P_{Cd}^{o^{0.27}} \quad (\Omega cm) \tag{6.3}$$

where P_{Cd}^{o} is in mbar.

Annealing in Cd or Te will adjust the stoichiometry of the CdTe matrix, introducing either Cd or Te vacancies. This could account for the increase in ρ after annealing in Cd, since this would introduce donors compensating the p-type conductivity due to phosphorus. It was thought that the introduction of excess Cd

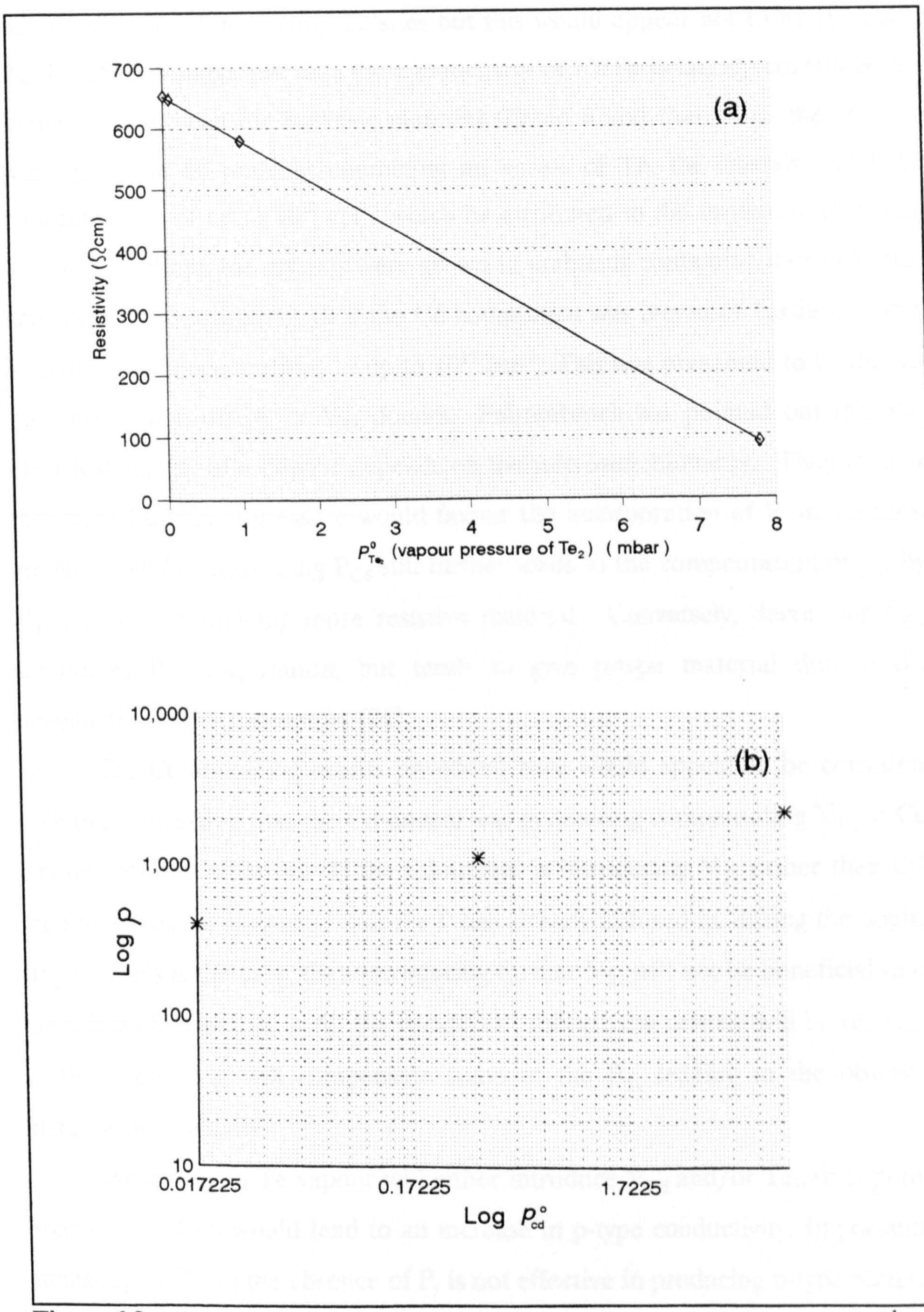


Figure 6.8 .. Dependence of CdTe:P resistivity on Cd/Te partial pressure in the 2nd stage of the doping process: (a) ρ vs P^o_{Te}, (b) Log ρ vs. Log P^o_{Cd}.

might encourage P to occupy Te sites but this would appear not to be the case. Zanio [25] has suggested that the conductivity of CdTe is largely controlled by native defects, even for extrinsic material. Zanio found that when the crystals were grown in an ambient containing an excess of Te, the crystals had hole concentrations of up to 10^{16} cm^{-3}, which he attributed to the formation of either V_{Cd} or Te_i. When the crystals were grown in ambients containing more Cd, the crystals became insulating, or if the Cd component was increased further, n-type with electron concentrations of up to 10^{17} cm^{-3}. This was presumed to be due to the introduction of Cd_i or V_{Te} donors. Fahrenbruch has pointed out that the electrical activity of a dopant depends on the microstoichiometry. Thus while a moderate Cd partial pressure would favour the incorporation of P on Te sites, yielding high N_A, increasing P_{Cd} still further leads to the compensation of p_{Te} by V_{Te} and/or Cd_i yielding more resistive material. Conversely, decreasing P_{Cd}, suppresses P incorporation, but tends to give p-type material due to the introduction of V_{Cd} acceptors [26].

The Cd-annealing results presented here would appear to be consistent with this, suggesting that the Cd-anneal was generating compensating V_{Te} or Cd_i centres into the material. If the Cd-anneal is introducing V_{Te} rather than Cd_i, then these results suggested that the P has already diffused in, during the doping stage. If this is the case, then introducing further V_{Te} will not be beneficial since there is no P available to fill the vacancies. Indeed, the reverse will be the case, as the excess V_{Te} will compensate some of the P_{Te} leading to the observed increase in resistivity.

Annealing in Te vapour will either introduce V_{Cd} and/or Te_i, or suppress excess V_{Te}. Both would lead to an increase in p-type conductivity. Importantly, annealing in Te, in the absence of P, is not effective in producing p-type material [24] with conductivity as high as measured here. The results therefore, suggest that, infact, the effect of the Te-anneal is to reduce the concentration of V_{Te} and

thus reduce the level of compensation. It will also be the case, of course, that V_{Cd} will be introduced increasing the acceptor density still further. The apparently linear plot of resistivity versus Te vapour pressure is consistent with an equilibrium constant expression for conductivity containing the term $[V_{Cd}]/P_{Te}$.

6.4. Properties of PGD CdTe:P

Solar cell performance is directly related to material properties; higher semiconductor conductivity generally leads to better performance and structural defects usually introduce problems with degradation [9]. The technological requirement of doping CdTe reproducibly, both n- and p-type, while maintaining control of the material resistivity is severely hindered by autocompensation effects which inhibit the process of compound doping [10]. Our plan has been to mount an extensive investigation of CdTe:P to reveal the reliability of PGD processes.

6.4.1. Structural Properties

6.4.1.1. Surface Composition

EDX analysis was used as a surface monitoring technique after each doping stage. By using different energies for the electron beam, different ranges of penetration can be reached. As the result of scattering events within the material, the range of electron penetration (R_e) is a function of the electron beam energy (E_b). Following the general expression derived by Kanaya and Okayama [11], that range is given by:

$$R_e = \frac{0.0276\,A}{\rho\,Z^{0.889}}\,E_b^{1.67} \quad (\mu m) \qquad (6.4)$$

where E_b is in keV, A is the atomic weight, ρ is the density of the material in gm

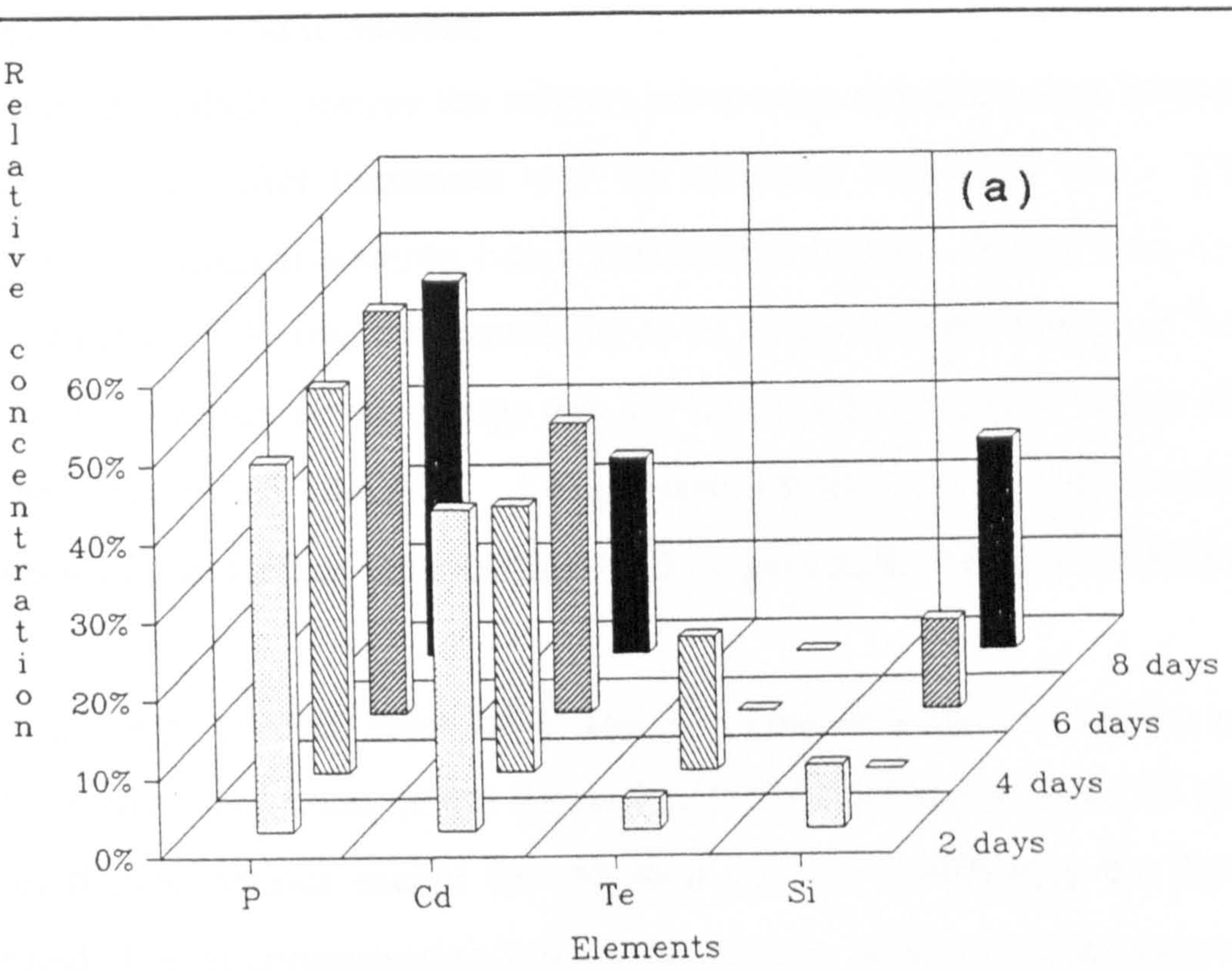


Figure 6.9 .. The relative percentage composition of elements on the CdTe surface after being treated in P for prolonged lengths of time; (a) for up to 0.45 μm and (b) for up to 3.7 μm from surface.

cm^{-2}, and Z is the atomic number.

Figures 6.9(a,b) portray the relative percentage distribution of elements on the CdTe surface, after treatment in P for different lengths of time. The two figures are for different electron beam penetration depths. Figure 6.9a, is for an effective depth of 0.45 μm, corresponding to an electron beam energy of 7.5 KeV. Figure 6.9b, (electron beam energy was 25 KeV) is for a much deeper electron beam penetration of ~3.7 μm. Comparison of the two figures provides an impression of the surface composition, and in particular, the P distribution with depth.

The high concentration of P and Cd observed for all doping periods, provides a clear indication of the formation of Cd_2P_3. Unexpectedly Si appeared after all doping periods except for the four day run which was the first to be performed. The Si concentration tended to increase with both the run order (all runs were performed using the same apparatus settings) and prolonged doping time. The presence of the silicon can be attributed to the attack by phosphorus compounds on the silica glass of the reactor tubes.

Therefore, the lowest resistivity that is shown in figure 6.3 (for the four day doping run) may be correlated to doping order, suggesting that undesired impurities, like Si, increase compensation. This, of course, leads to higher resistivity and lower free carrier concentration.

6.4.1.2. Pipe Diffusion

Cathodoluminescence (CL) microscopy was used to investigate the distribution of luminescent centers, which are associated with the presence of phosphorus, before and after doping of the CdTe. The phosphorus provides radiative recombination sites for electron-hole pairs produced by the electron beam, and thus the CL image gives the phosphorus distribution. An analysis of diffusion surfaces in P doped CdTe using the SEM/cathodoluminescence (CL)

technique revealed crystallographic defects, like sub-grain boundaries and dislocations, these being represented by areas of bright CL contrast (see figure 6.10). This differs from that observed in undoped CdTe, where the CL contrast is dark at crystal defects due to the occurrence of non-radiative recombination. The implication is that it is energetically favorable for the P atoms to segregate preferentially to crystal defects so altering the luminescence observed.

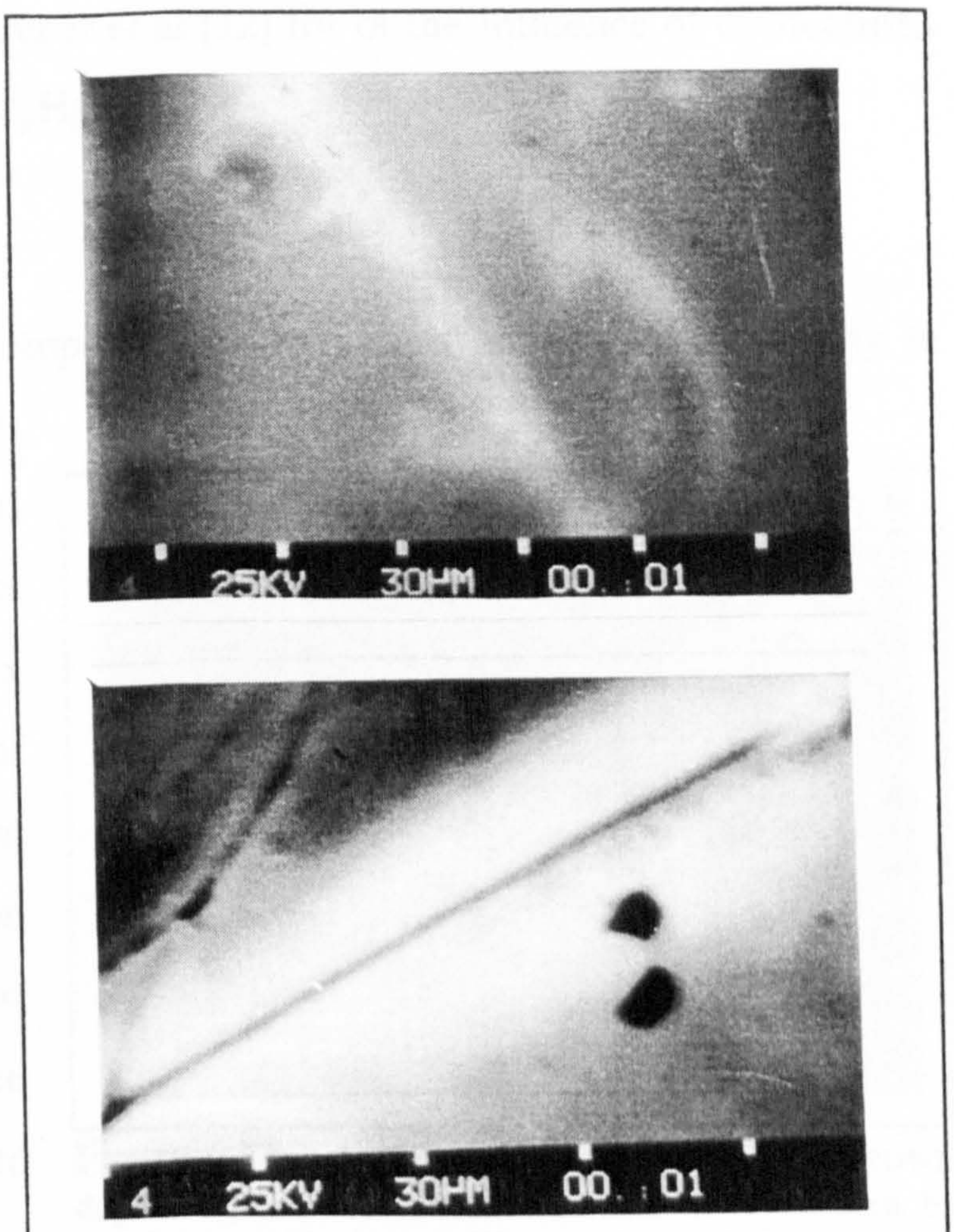


Figure 6.10 .. Micrographs of diffusion surfaces in P doped CdTe using the SEM/CL technique. Crystallographic defects play an important role in the PGD process.

By cleaving perpendicular to the surface, and then examining the spatial distribution of the CL contrast produced, it was possible to obtain an indication of the distribution profile of the dopant through the bulk of a doped CdTe sample. As expected bright CL contrast was imaged at and near the diffusion faces indicating high levels of P, but bands of similar contrast were seen to penetrate into the sample bulk. These bands follow grain boundaries running through the CdTe and provide support for the idea that impurities are preferentially segregated to crystal defects. The role of such defects in the diffusion process is thus seen to be very important, in that they provide a rapid mechanism for transport of P into the crystal bulk. This mechanism

is similar to that reported by Archer et al [12] for of the influence of dislocations on mercury diffusion in bulk $Cd_xHg_{1-x}Te$.

6.4.1.3. Precipitation

Precipitation and self compensation are natural effects of P impurity in during growth doped CdTe. Courreges et al reported that in their approach Hall effect measurements gave p = 6.3 x 10^{16} cm^{-3} which is about 5% of the composition [21] implying that most of the P was not on simple substitutional sites. Post growth doped CdTe:P examined in the TEM was found to contain dislocations decorated by precipitates, as in figure 6.11. The precipitates were found to contain phosphorus as determined by EDX, figure 6.12. Examination in cross-section revealed the variation in the defect microstructure with distance from the free surface. The complex tangle of dislocations illustrated in figure 6.13 is typical of the near surface region which is free of inclusions. However, at

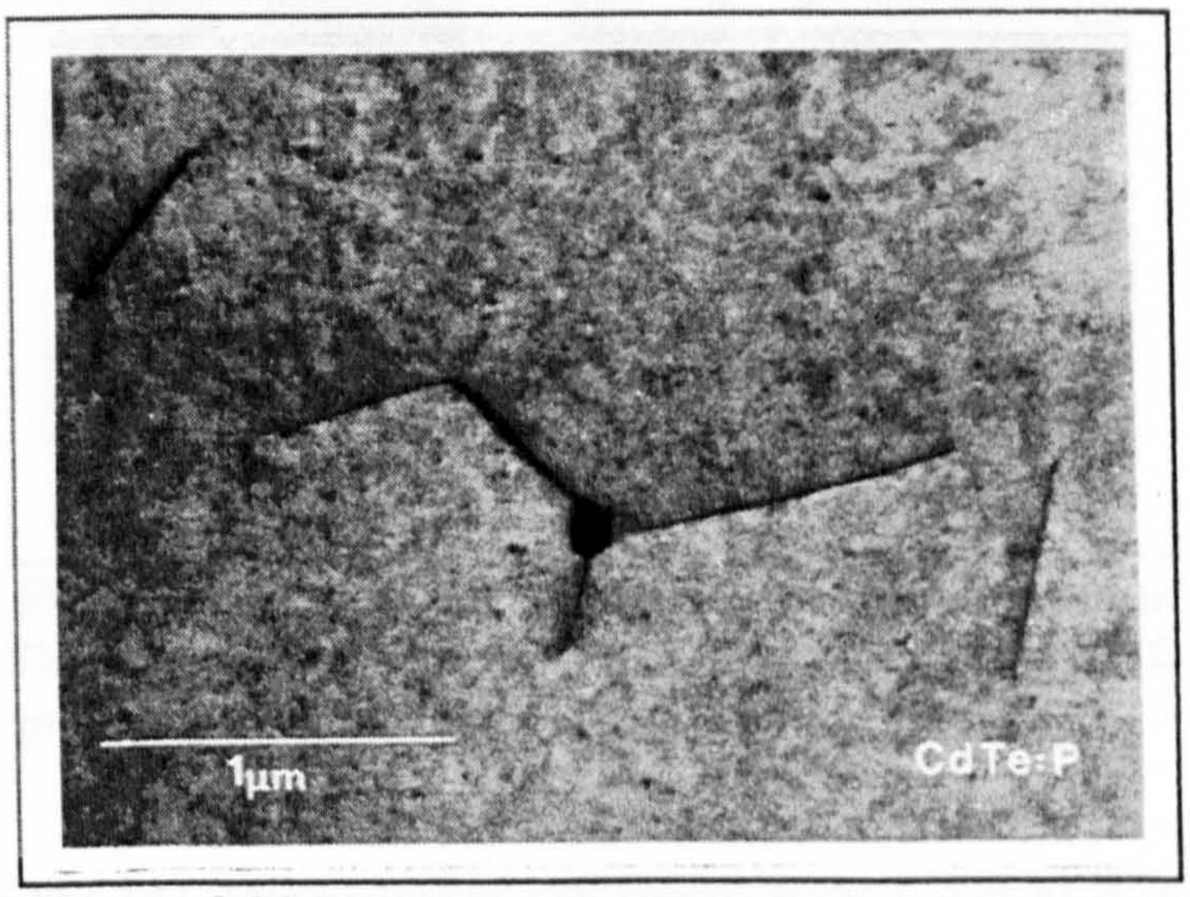


Figure 6.11 .. A TEM photographof a post growth doped CdTe:P. A dislocation that is decorated by precipitates.

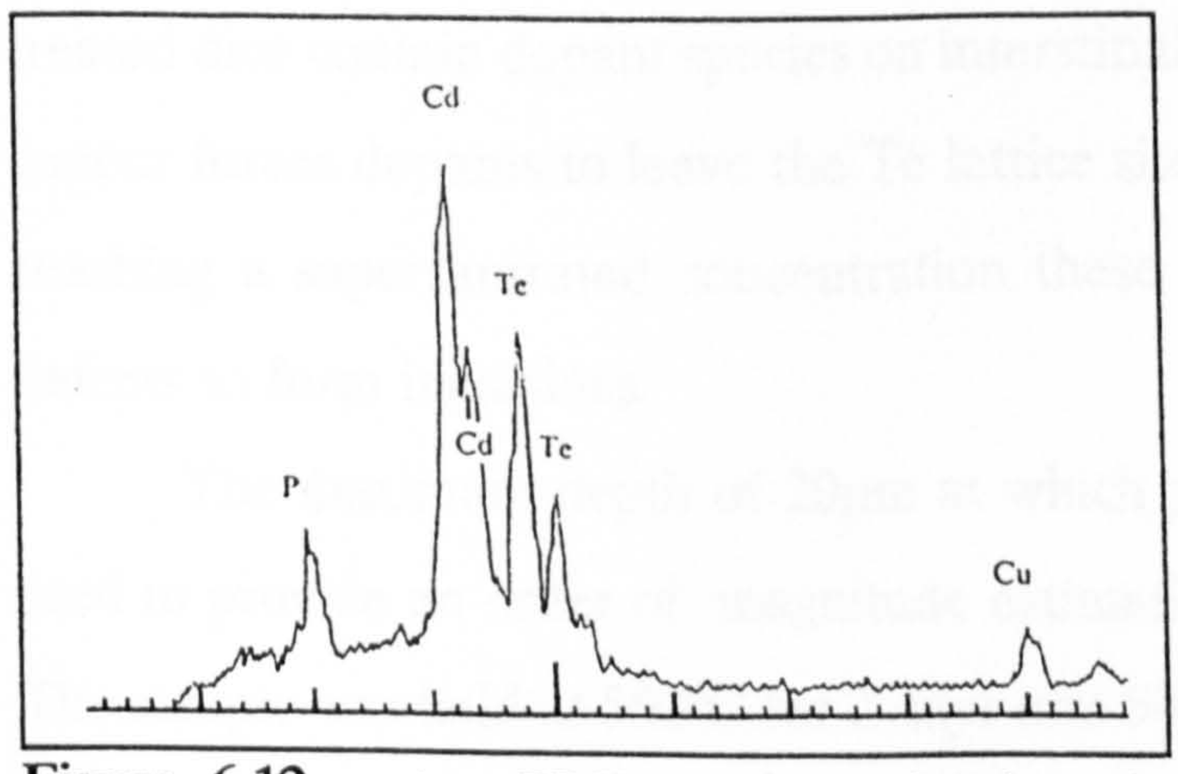


Figure 6.12 .. An EDX readout showing the composition of the precipitate that is shown in figure 11.

a depth of ~15 to 20 μm below the surface, inclusions which contained P similar to that shown in figure 6.11 were seen to decorate dislocations. No precipitates or inclusions were observed at a depth greater than about 20μm.

Since the dice were chemically polished and damage free before doping, it may be inferred that the near surface dislocation tangle is introduced by strains resulting from compound formation at the surface and the high concentration of P diffusing into the matrix, which is known, for example, to disrupt the crystal lattice during P diffusion in silicon [13,14]. Precipitates are presumably absent due to the high density of sinks. The absence of a high density of faults deeper within the dice allows precipitation to take place, in the following manner [15]. The P treated dice contain dopant species on interstitial and lattice sites. Annealing in Te vapour forces dopants to leave the Te lattice sites and become interstitial, and on reaching a supersaturated concentration these interstitials associate with native defects to form inclusions.

Figure 6.13 .. A representative TEM photograph of CdTe surface after being treated with P in the PGD process.

The maximum depth of 20μm at which precipitation was observed can be used to provide an order of magnitude estimation of the diffusivity of P in CdTe. The sample was held at 550°C for 2 days and 540°C for 7 days and hence; $D = L^2/t$ ~ 5×10^{-12} $cm^2 s^{-1}$.

6.4.2. Electrical Properties

6.4.2.1. Hall Data

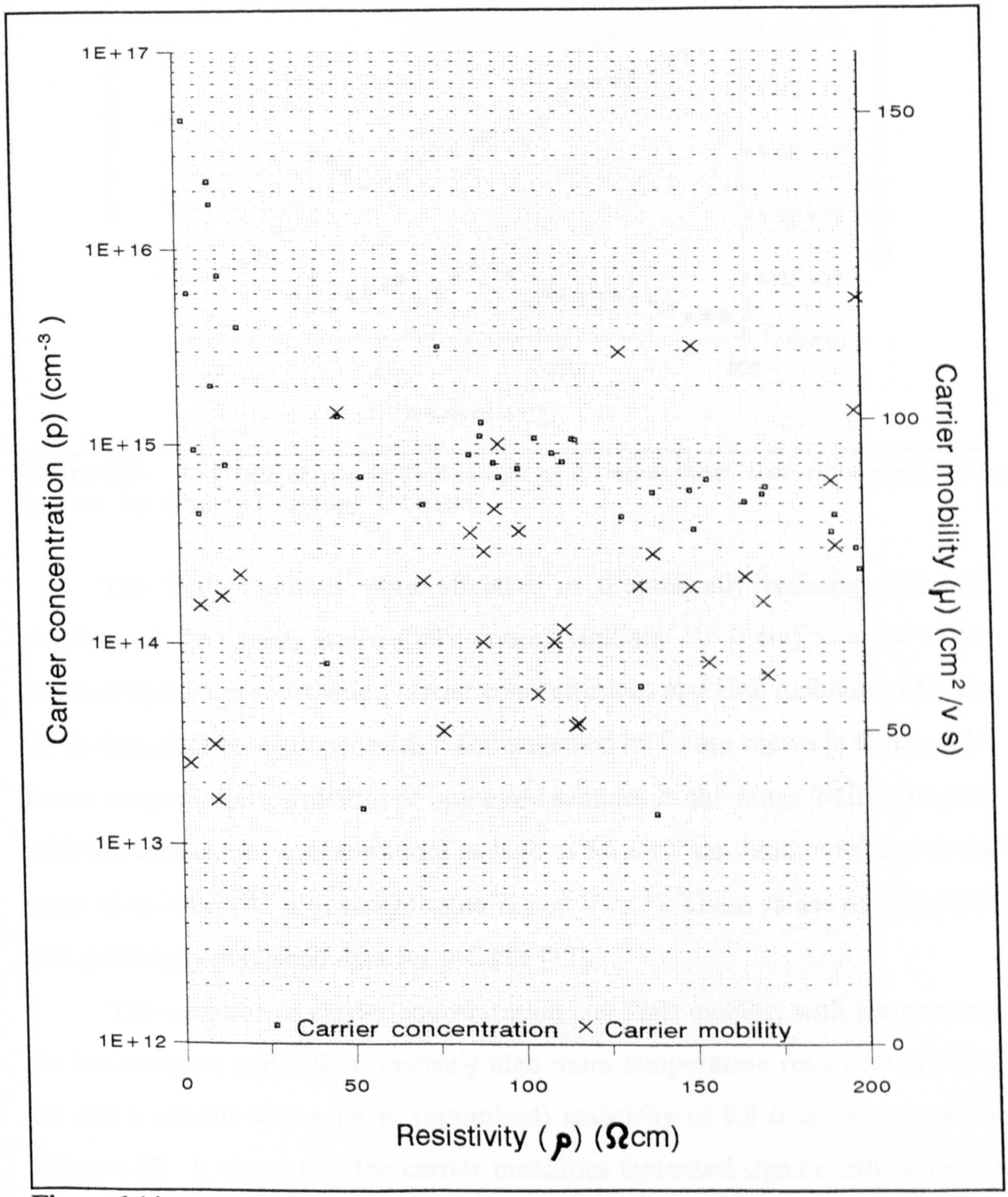


Figure 6.14 .. Room temperature resistivities, carrier concentrations and Hall mobilities of selected CdTe dice, after being doped with P and annealed in Te.

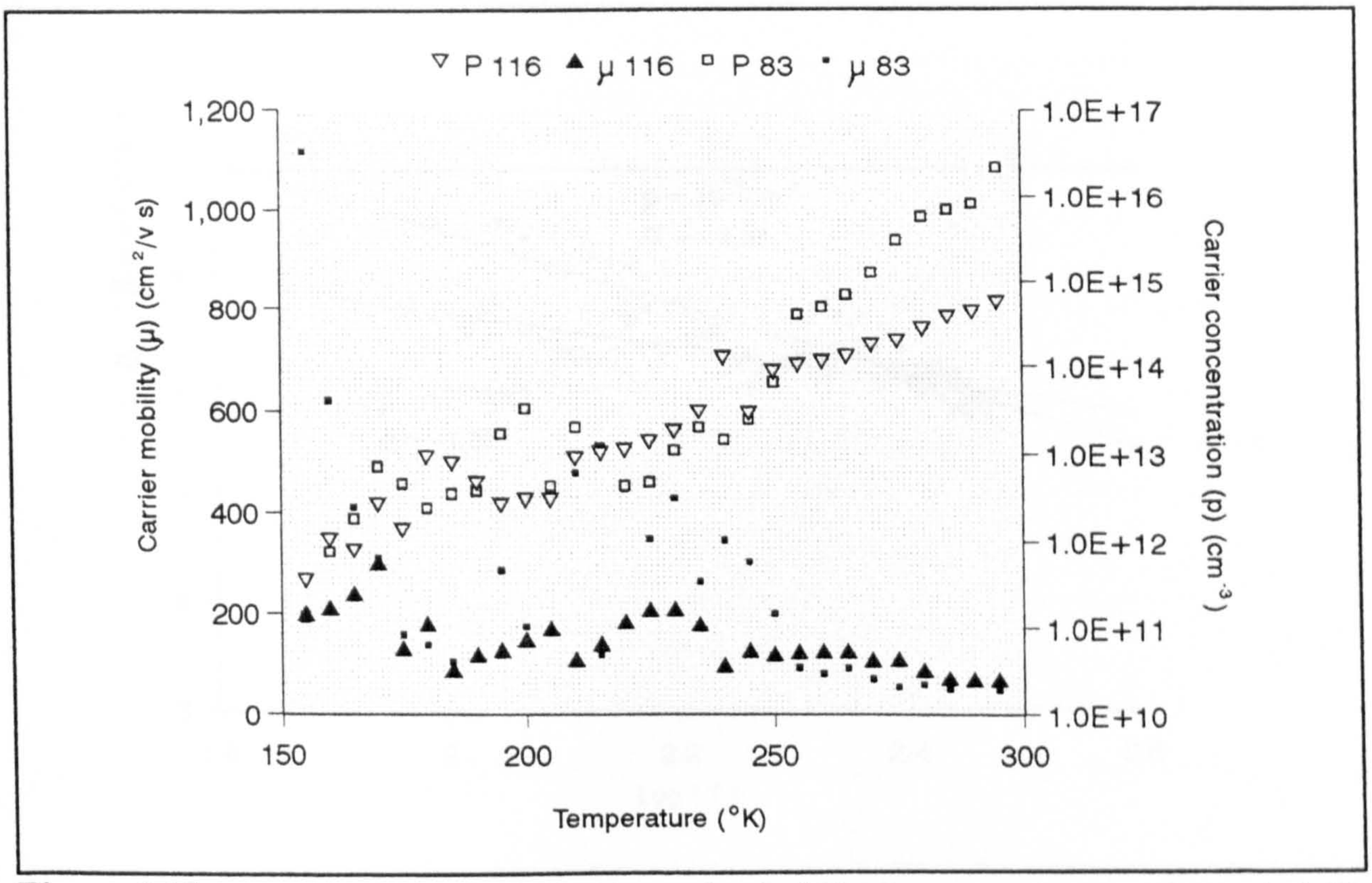


Figure 6.15 .. Hall data of two CdTe:P sample of different room temperature resistivities [ρ(83)= 9.8 Ωcm and ρ(116)= 171 Ωcm].

The PGD methods were effective in dramatically reducing the high resistivity of the vapour grown CdTe crystals (initially 10^8 Ω cm) to a few Ω cm. Room temperature resistivities, carrier concentrations and Hall mobilities of many CdTe dice, after being doped with P and annealed in Te are shown in Figure 6.14. Room temperature resistivities of optimised samples in the range 2-10 Ω cm were achieved with carrier concentrations as high as $5.5 \times 10^{16} cm^{-3}$ and mobilities in the range 45 to $100 cm^2 V^{-1} s^{-1}$ (average value 72 $cm^2 V^{-1} s^{-1}$). These values compare well with previously published data for p-CdTe [17].

The variation in carrier concentration and Hall mobility with temperature for two samples; one with a relatively high room temperature resistivity of 171 Ω cm and a second with a lower (optimised) resistivity of 9.8 Ω cm are shown in Figure 6.15. It shows that the carrier mobilities increased significantly when the temperature was reduced, reaching values as high as 1150 $cm^2 V^{-1} s^{-1}$.

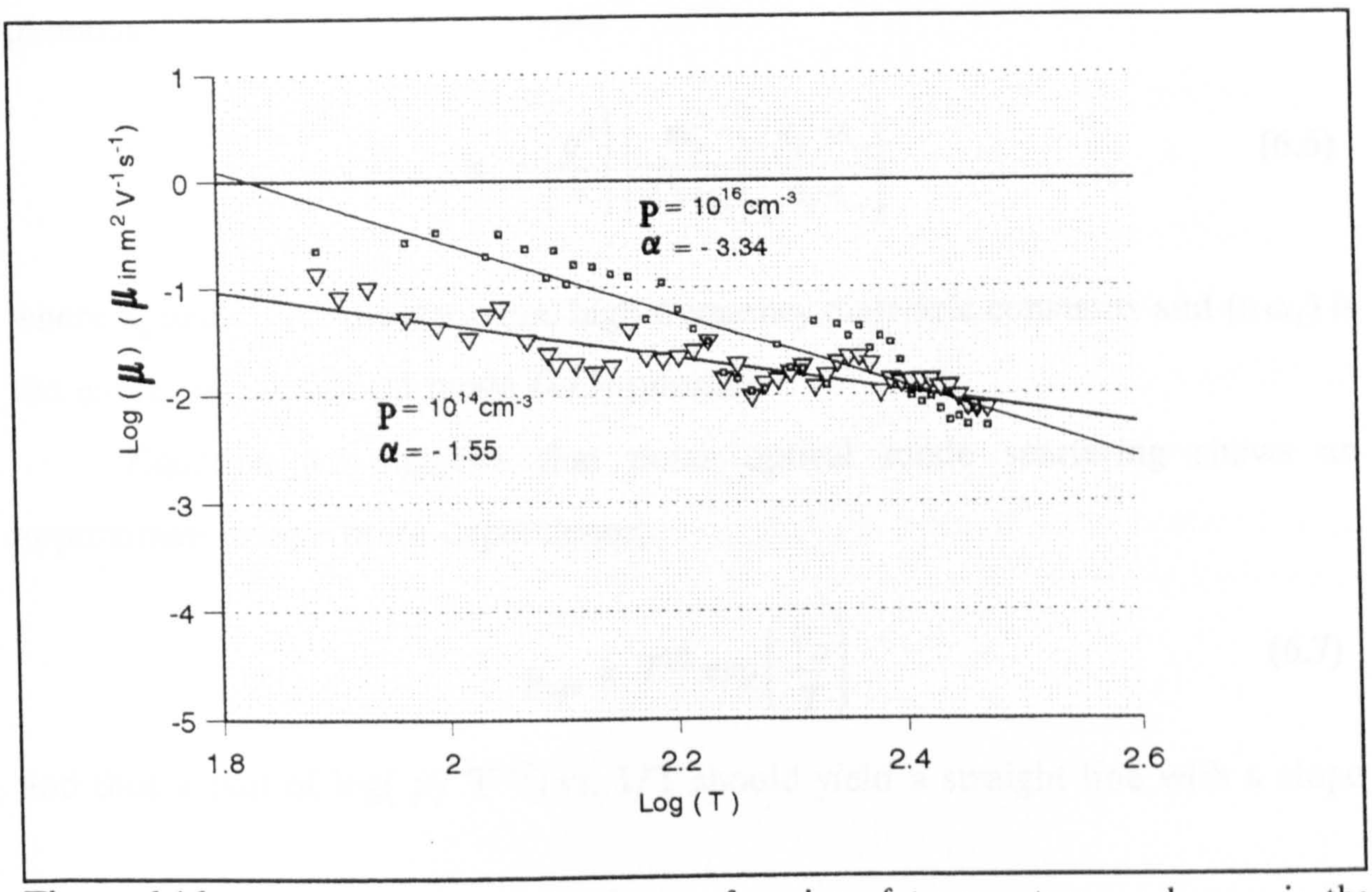


Figure 6.16 .. Hole mobility in CdTe:P as a function of temperature ; where α is the temperature proportionality dependence factor.

The detailed temperature dependence of the mobility of the two samples is shown in Figure 6.16 which reveals that the hole mobility in lower carrier concentration semiconductor, followed a $T^{-3/2}$ proportionality, indicating that lattice scattering was the principal limiting process. However, the more highly doped samples showed a different and stronger temperature dependence, ($T^{-3.3}$ on the log (μ) vs. log (T) plot of Figure 6.16). Such a strong dependence on temperature is often associated with polar optical mode scattering. This is described by an equation of the form:

$$\mu(T)_{opt} = \frac{1}{2\alpha\omega_1} \cdot \frac{q}{m_p^*} \cdot \frac{8}{3\sqrt{\pi}\sqrt{z}} \Psi(z)\{e^z - 1\} \qquad (6.5)$$

where z is the ratio of the Debye temperature (θ_D) to the lattice temperature (i.e. $z = \theta_D / T$), $\Psi(z)$ is a factor $\simeq 1$ for the temperature range used here, α is the coupling constant for the interaction between a charge carrier and the optical mode

phonons:

$$\alpha = \left[\frac{q^2}{\hbar}\right]\left[\frac{m_p^*}{2\hbar\omega_1}\right]\left[\frac{\epsilon_s - \epsilon_\infty}{\epsilon_s \epsilon_\infty}\right] \qquad (6.6)$$

where ε_s and ε_∞ are the static and high frequency dielectric constants and $(\hbar\omega_1)$ is the energy of the optical mode (LO) phonon.

Equation 6.5 suggests that polar optical mode scattering shows an approximate temperature dependence;

$$\mu_{opt} \alpha T^{1/2} \exp\left(\frac{\theta_D}{T}\right) \qquad (6.7)$$

and thus a plot of log(μ/ $T^{1/2}$) vs. 1/T should yield a straight line with a slope

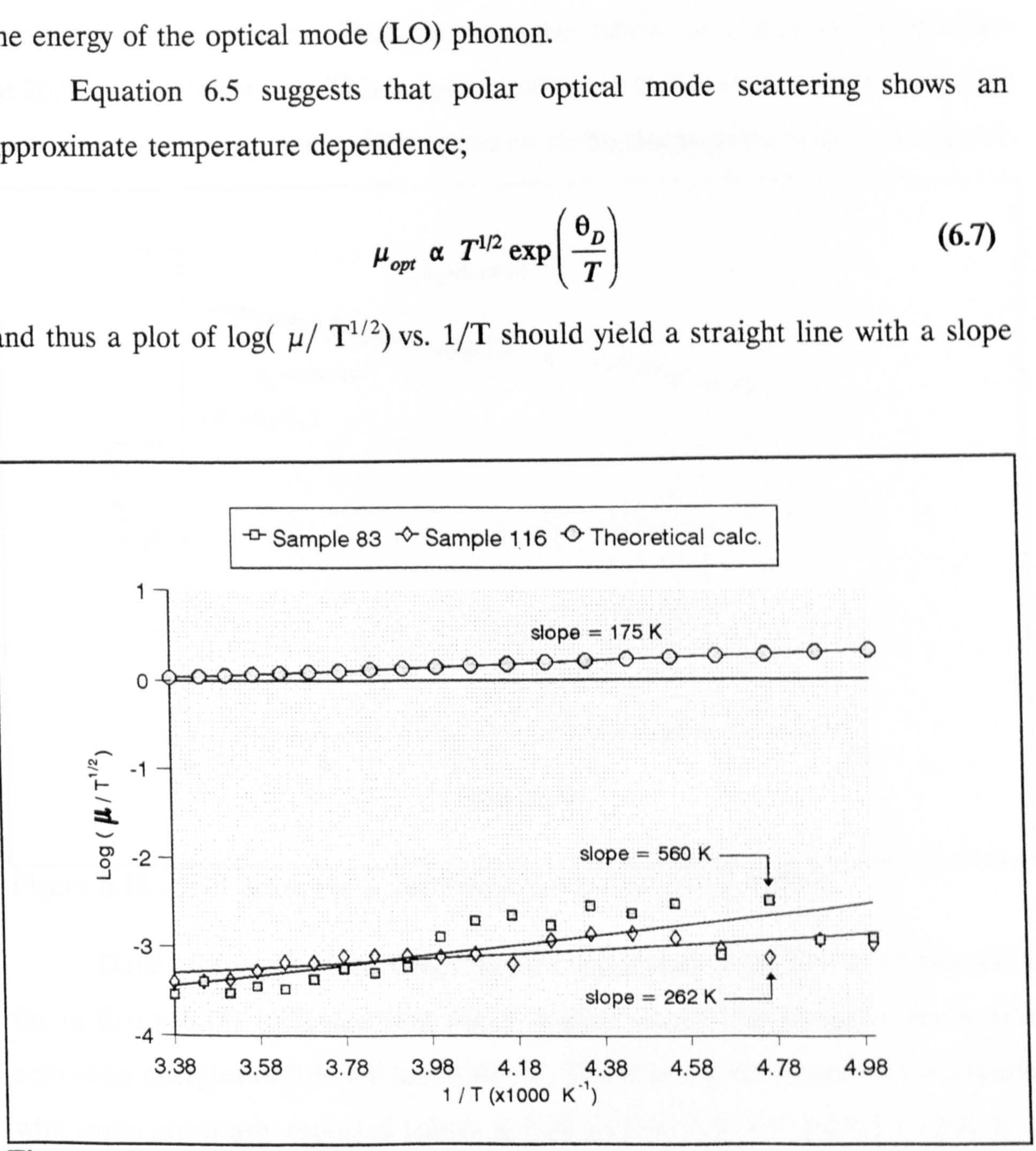


Figure 6.17 .. The charge mobility in the higher carrier concentration sample together with a theoretical calculation of the polar optical scattering limited mobility both plotted versus temperature.

equal to θ_D, the Debye temperature.

The data have been replotted in Figure 6.17 together with a theoretical calculation of the polar optical scattering limited mobility (for CdTe, θ_D = 158 K, $\hbar\omega_1$ = 23.5 meV, ε_s = 10.2 , ε_∞ = 7.2). The graph shows reasonable straight lines but with absolute magnitudes some 10^3 times smaller than expected. The sample curves had steeper slopes at 560K for the higher carrier concentration sample than at 262K for the lower one. This suggests that it is a rather more complex situation with several scattering mechanisms operative in the temperature range investigated.

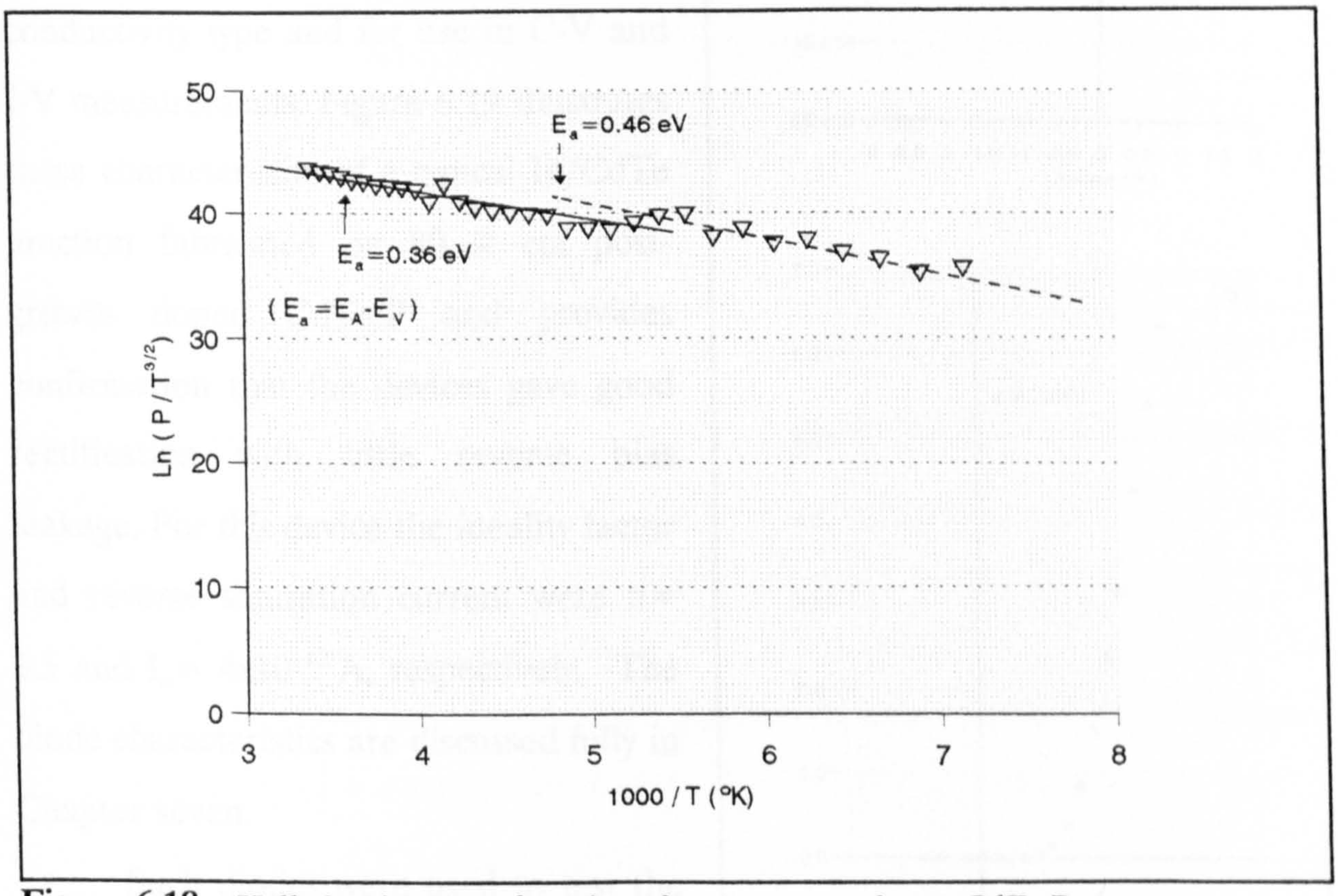


Figure 6.18 .. Hall density as a function of temperature for p-CdTe:P.

Detailed analysis of the temperature dependence of the Hall coefficient data (as in figure 6.18) indicated that the P doping resulted in acceptor levels with activation energies of 0.36 eV and 0.46 eV. These are rather deep but correspond with some previously reported values ie 0.38 eV[18], 0.32 eV and 0.5 eV[19]. It is likely that in reality there is more than one P-related level and that only the deeper centres are active in the temperature range investigated.

6.4.2.2. Uniformity of Doping

Indium metal was deposited by evaporation on mechanically and chemically polished CdTe surfaces to fabricate In/CdTe Schottky diodes. Au was used to form the back contact of all the diodes. These diodes were fabricated both as an initial means of confirming conductivity type and for use in C-V and I-V measurements. Figure 6.19 illustrates these characteristics of a typical In/CdTe junction fabricated on 80 Ω cm post-growth doped CdTe:P and provides confirmation that the devices gave good rectification with little reverse bias leakage. For this device the ideality factor and reverse saturation current were n= 3.5 and $I_o = 4x10^{-12}$ A, respectively. The diode characteristics are discussed fully in Chapter seven.

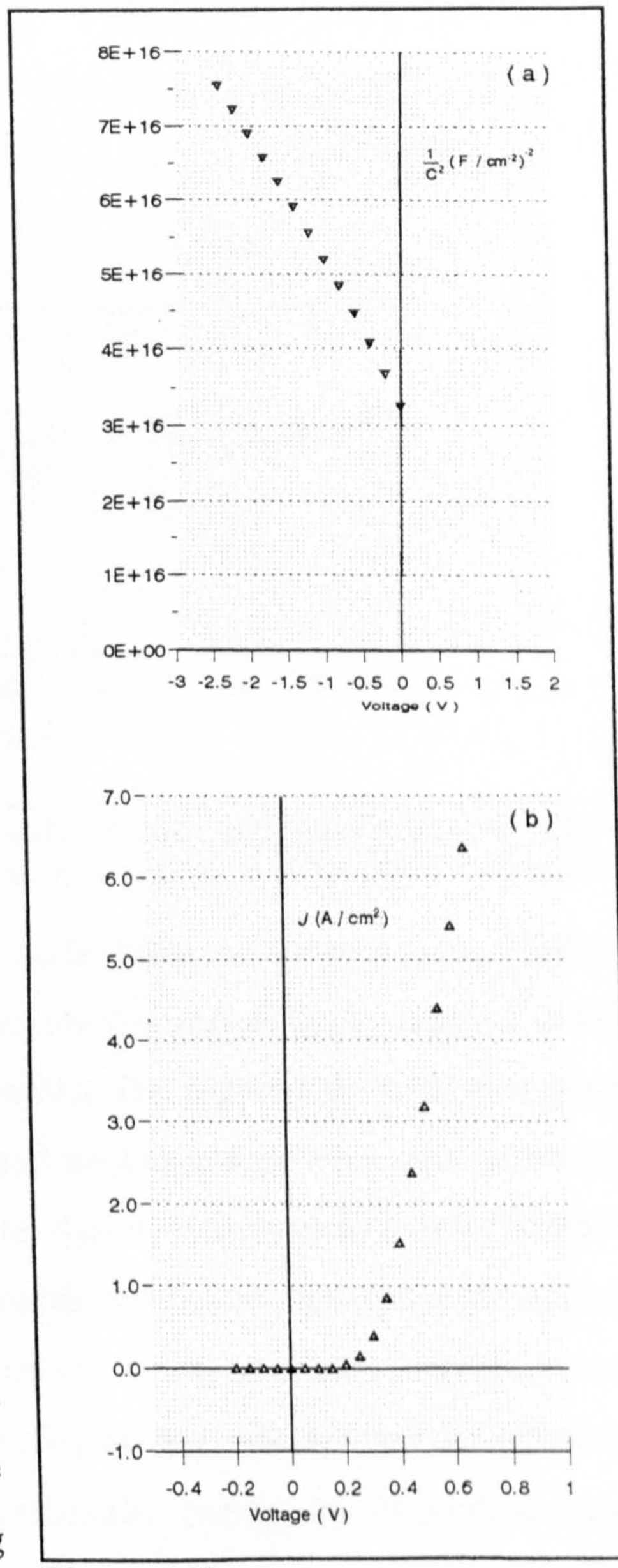


Figure 6.19 .. (a) C-V and (b) I-V characteristics of a typical In/CdTe junction, that was used in the determination of the impurity diffusion profile in PGD CdTe:P.

Such diodes were used to test the uniformity of the impurity diffusion profile in post-growth doped CdTe:P dice, using a step etch and measuring technique. The profile C-V test was carried out by chemically etching a layer of the semiconductor and then recording the C-V characteristic to obtain a value of the net acceptor concentration ($N^-_A - N^+_D$) at that depth. The results of these etching

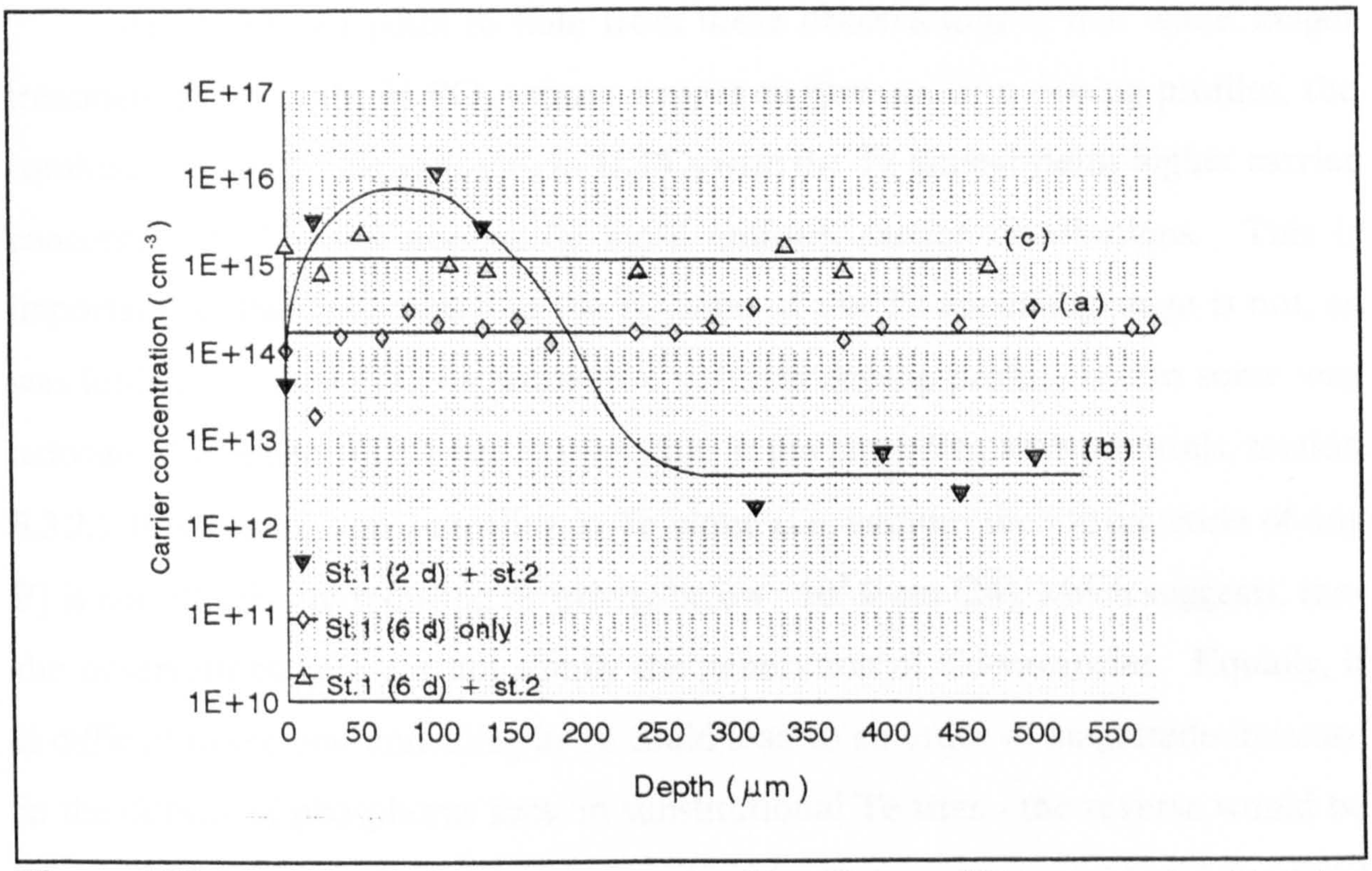


Figure 6.20 .. The $(N^-_A - N^+_D)$ concentration profiles of three different samples; (a) 6 days doped - not annealed, (b) 2 days doped & annealed, and (c) 6 days doped & annealed.

experiments are presented in figure 6.20, which shows the concentration profiles of three different samples; (a) doped (6 days) but not annealed, (b) doped (2 days) & annealed, and (c) , doped (6 days) & annealed. The depths were measured using a Tencor Alfa-Step 2000 surface profiler and measurements were taken down to ~500μm, approximately half way through the dice. It is quite clear that for sample (a) the net acceptor concentration is uniformly distributed throughout the tested depth. The I-V characteristics near the surface of this specimen were poor but improved dramatically deeper into the dice. This profile indicates that the diffusion of P into the CdTe dice takes place principally during the orthophosphoric heat-treating stage. For sample (b), the $(N^-_A - N^+_D)$ distribution profile, after an initial rise decreased with depth until it reached a uniform doping level after ~1/5 of the over-all dice width, indicating that diffusion through the sample had not equilibrated. Finally, sample (c) provides an example how uniform the profile becomes after 6 days doping followed by a 7 day Te anneal.

An interesting point to note from these observations is that while longer treatment times in the H_3PO_4 vapour appear to give uniform doping profiles, the combination of a longer exposure to H_3PO_4 with the Te anneal yields higher carrier concentrations but not necessarily more uniform carrier distributions. This is important, in that it implies that the function of the Te-annealing stage is not, as was initially thought [24], to promote a uniform doping profile, but in some way activates the dopant. (This was also implied in the annealing ambient trials, section 6.3.2.). It is known, that annealing in Te alone (i.e. without the introduction of any P) is not effective in reducing resistivity below ~10^3 Ω cm [24], which suggests, that the observations here are not simply the generation of Cd-vacancies. Equally, it is difficult to see how annealing *in Te* could lead to an order of magnitude increase in the density of phosphorus ions on substitutional Te sites - the reverse would be expected. These results suggest that in fact the Te anneal is enabling interstitial phosphorus to form complexes possibly with Cd vacancies, so as to dramatically increase the net acceptor density either by the creation of new acceptor centres or possibly by a reduction in the compensating donor concentration.

6.5. Phosphorus Diffusion Mechanism

Diffusion, defined as the migration of particles due to their random thermal motion, is a natural process when two different materials are brought together. Such migration may be enhanced in solids by increasing the internal energy of materials under study, i.e. by raising the temperature. Generally, diffusion rates are significantly affected by the defect content of the host material and can either enhance or impede diffusion processes. In the present case, pipe diffusion effects have been shown to play a major role in conveying the phosphorus into the crystalline bulk. However, it has also been shown that the phosphorus is not necessarily activated as an acceptor impurity until after an extensive annealing

treatment in Te.

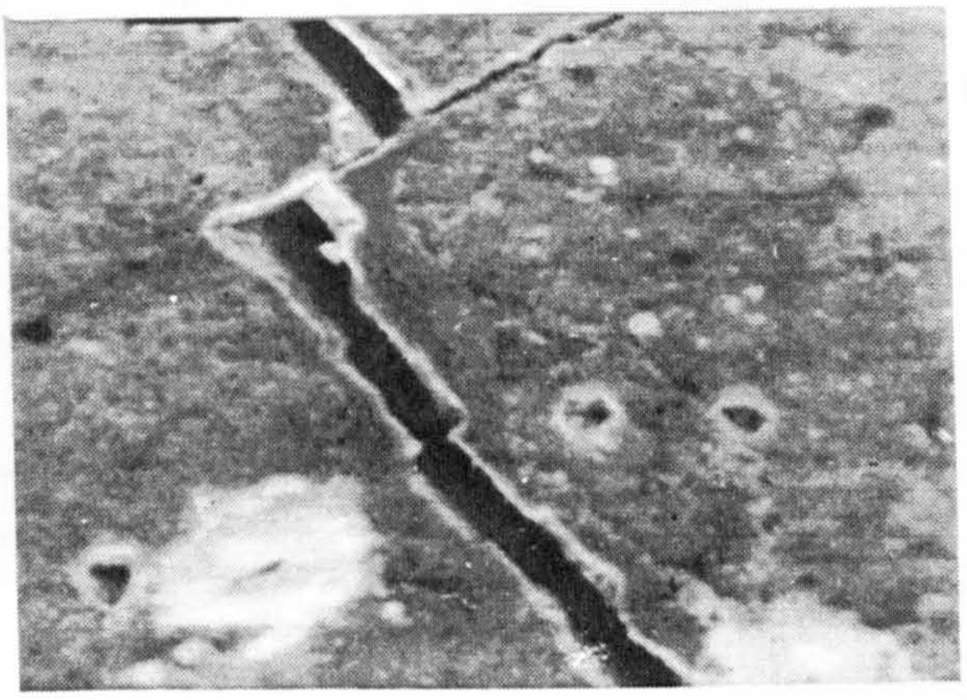


Figure 6.21 .. (a) SEM photo of dice surface after being treated in the 1st stage of the PGD process. (b) EDX output of elements detected on the surface.

Although the doping procedure developed in this study superficially appears to be a two stage "coating + drive-in" technique, the process has been shown to be not as straight forward as it appears. After heating CdTe in H_3PO_4 vapour, P is deposited on the surface and then probably undergoes a chemical reaction with Cd to form Cd_3P_2. Figure 6.21a shows an SEM micrograph of the surface of a CdTe sample after treatment in H_3PO_5 vapour. The extensive surface deposits show how thick the P coat can become. An EDX analysis, (figure 6.21b), of such a layer strongly suggests that it consists mainly of Cd and P. (This is more likely to be Cd_3P_2 + P). The surface deposits were examined in more detail, by exposing CdTe dice to H_3PO_4 vapour without heating (during the usual doping procedure, the dice are maintained at ~550°C). The dice were then subsequently heated to 500°C and examined in the SEM. The surface of such a CdTe sample is shown in Figure 6.22a and displays a uniform distribution of 20μm features. Analysis by EDX (Figure 6.22b) showed that the features contained Te whereas the background did not. This suggested that Te was being preferentially removed from the surface.

It was also observed that following CdTe doping trials, there were deposits

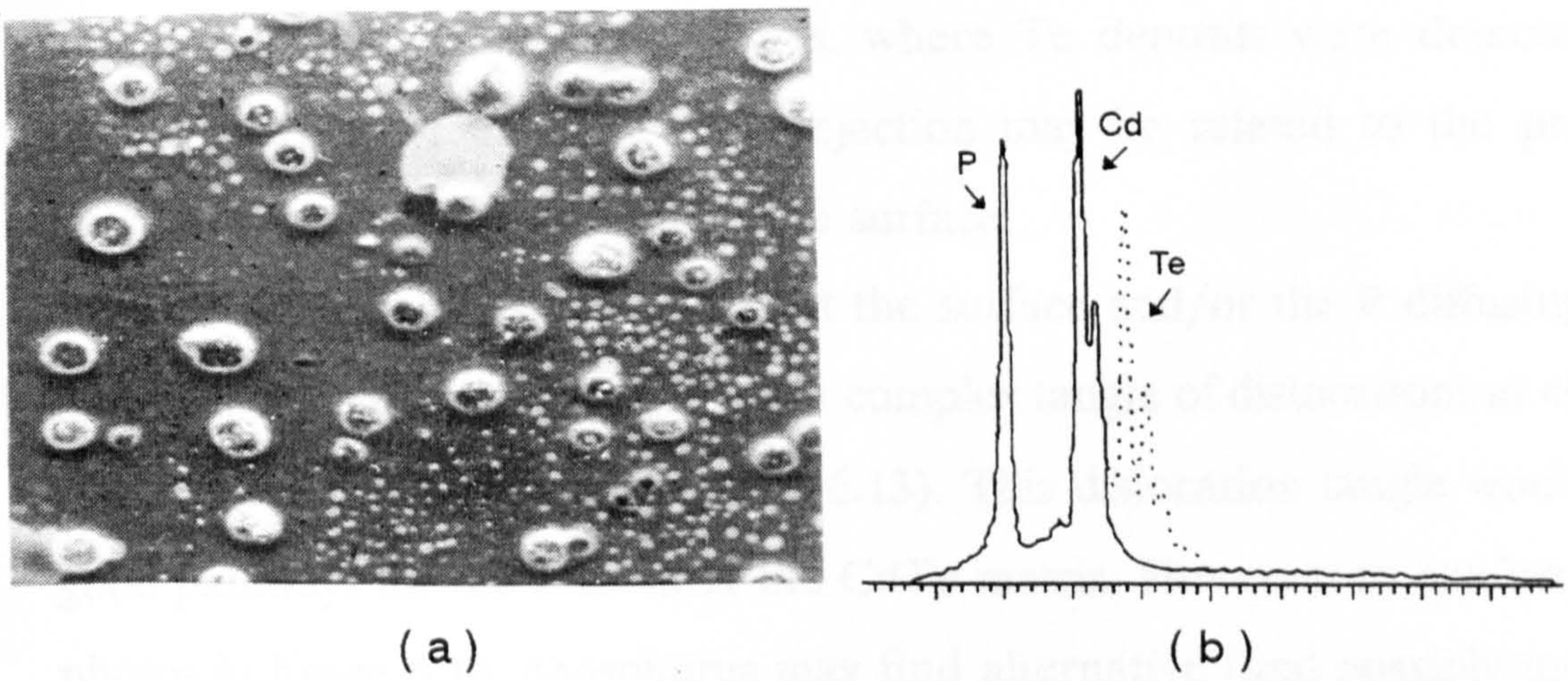


Figure 6.22 .. (a) SEM photo of H_3PO_4 treated CdTe showing 20μm features on the surface. (b) An EDX output of elements existing on dice surface, where (—) between (— + - -) on the features.

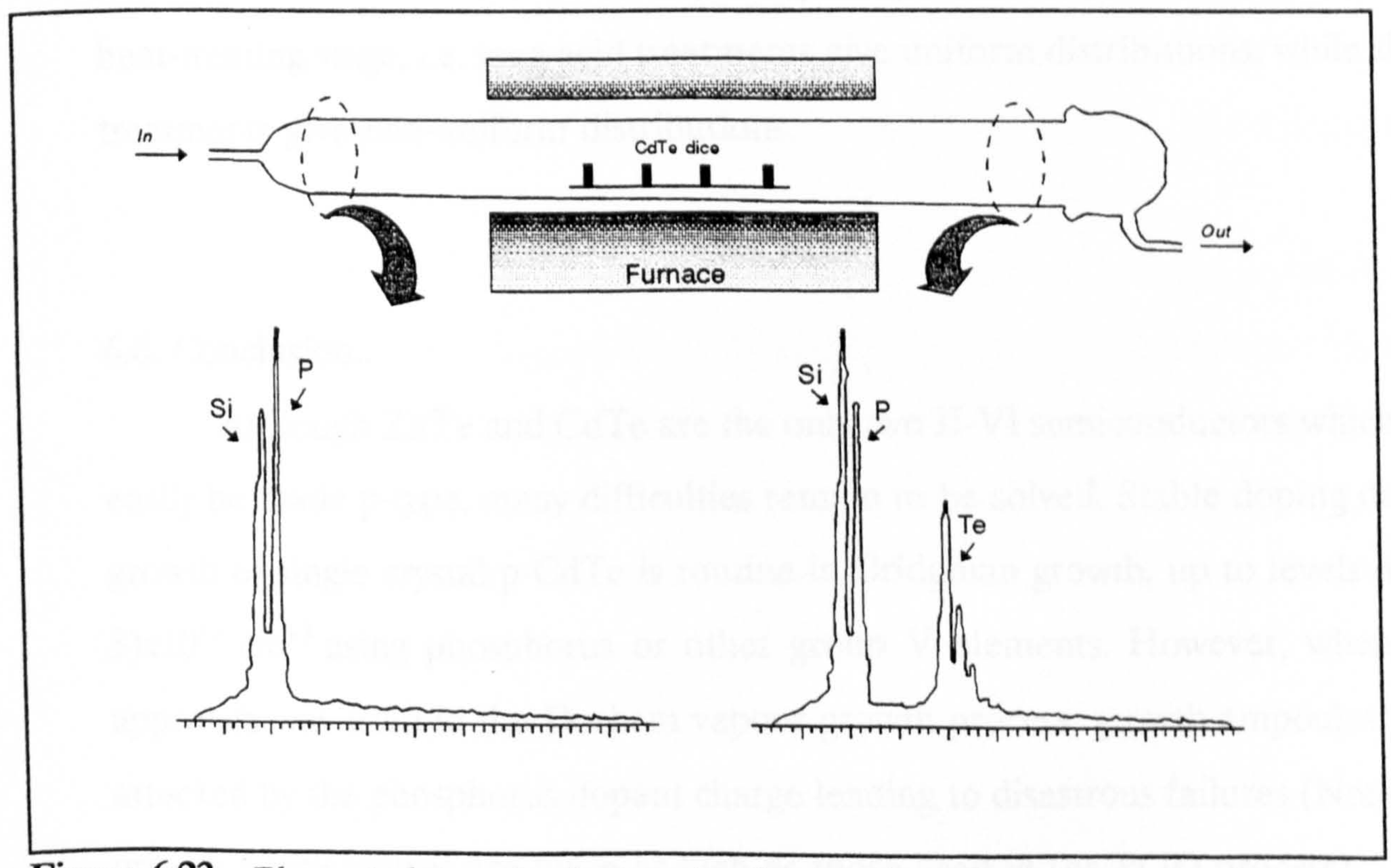


Figure 6.23 .. Elements detected at both ends of a reaction tube following use in an open tube doping treatment for CdTe dice.

on the inside surface at both ends of the reactor tube. At the inlet side, these were white in colour and were found to consist principally of P + Si. However, at the exhaust side, the deposits were grey/black in colour and when analysed by EDX

were found to contain Te as well as P and Si (Figure 6.23). Similar effects were obtained in the sealed doping tubes, where Te deposits were detected on the internal surface of the tube. The rejection may be related to the preferential formation of Cd_3P_2 compound on the surface.

The formation of the Cd_2P_3 at the surface and/or the P diffusing into the matrix introduces strains that result in complex tangle of dislocations at or near the surface region (illustrated in Figure 6.13). This dislocation tangle would provide good pathways for the P to enter the CdTe matrix. However, as confirmed by CL photos in figure 6.10, phosphorus may find alternative (and possibly more rapid) ways through by following the polygonisation walls and other crystal defect features. Moreover, the carrier concentration profile (as in figure 6.20) suggests that P diffusion into the CdTe dice takes place principally during the orthophosphoric heat-treating stage, i.e. long acid treatments give uniform distributions, while short treatments give non-uniform distributions.

6.6. Conclusion..

Although ZnTe and CdTe are the only two II-VI semiconductors which can easily be made p-type, many difficulties remain to be solved. Stable doping during growth of single crystal p-CdTe is routine in Bridgman growth, up to levels of (2-3)x10^{17} cm^{-3} using phosphorus or other group V elements. However, when this approach was tried in the Durham vapour growth process, growth ampoules were attacked by the phosphorus dopant charge leading to disastrous failures (Note that growth temperatures are twice as high as those used in the PGD process).

It has been necessary, therefore, to carry out the doping process, in two stages. In the first stage a thin layer of a mixture of Cd_3P_2+P in various proportions, was deposited on the top of the sample. During the process acceptor impurities were presumably incorporated into the CdTe by in-diffusion from the

doping layer. Annealing, as a second stage, in Te activated the dopant and possibly adjusted the stoichiometry of the CdTe matrix by introducing vacancies.

The optimum treatment for producing conductive p-type CdTe crystals investigated here was found to be: 1) heating in saturated H_3PO_4 vapour at 550°C for 4 days using the 'open tube' method and then 2) annealing in Te vapour at 400 °C for 5 days. Better results were achieved using a fresh system and a continuous saturated flow of acid vapour. Resulting samples had hole concentrations of up to $5.5x10^{16}$ cm^{-3} at room temperature, corresponding to resistivities in the 10 Ωcm range. However, better results may be achieved if containers other than silica tubes are employed since the H_3PO_4 has been found to attack the silicon and this may lead to contamination. Although orthophosphoric acid is less dangerous and cheaper than other P sources materials which did not, in anycase, provide better results, those sources or others should be examined further in the open tube method. Further modifications to the system might also be envisaged for example by using a double zone furnace.

It was inferred that annealing in Cd or Te vapour after treatment in H_3PO_4 vapour influenced the conductivity by changing the intrinsic vacancy concentration rather than influencing phosphorus site occupancy. In this way annealing in Te introduced additional acceptors (or reduced compensating donors) contributing to p-type conductivity while annealing in Cd introduced donors compensating the conductivity due to phosphorous-related acceptors.

C-V carrier concentration depth profiling showed that an extended treatment in H_3PO_4 facilitates the uniform diffusion of phosphorus into the bulk. Electron microscopy indicated that the PGD process was assisted by pipe diffusion. Hall and C-V measurements confirmed the material to be p-type and hence suitable for the fabrication of solar cell devices.

6.7. References

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Chapter VII

In/CdTe Schottky Diodes

7.1. Preface

The deposition of metal on cadmium telluride has been used for a long time to produce either ohmic or rectifying contacts. Devices have been made in this way for nuclear radiation detectors [1] electroluminescent diodes [3] and solar cells [4]. Metallic contacts used in the fabrication of semiconductor devices ordinarily range from electropositive metals such as In to the most electronegative elemental metal, namely Au. However, according to the Schottky model, all metals should create a barrier when contacted to p-CdTe, simply because there is no elemental metal with a work function high enough to be comparable to the electron affinity of CdTe. It is an indication of the confusion in the literature that gold has been claimed to form both rectifying and ohmic contacts to p-type cadmium telluride, irrespective of the magnitude of the work function of gold.

In this chapter we shall describe the use of In as a rectifying contact to p-CdTe, which was initially used as a preliminary indication of CdTe type conversion following PGD. In/CdTe Schottky diodes were also useful in the programme to optimise ohmic contacts to phosphorus doped CdTe and as a means of characterising the p-CdTe in terms of the net ionised acceptor density. Previously published results are described as a preface to this chapter, which is followed by an account of the results of this investigation.

7.2. Rectifying contacts to p-CdTe

In this section some published results on the subject are summarised. This is done by collecting reported values of the barrier heights made by various

metals to p-type CdTe and highlighting the variations introduced by different surface preparations before deposition of the metal.

The barrier height (ϕ_B) is like a finger-print for each diode. The conventional Schottky model indicates that the barrier height at a metal-semiconductor interface should be highly dependent on the work function of the metal and therefore large variations in φ_B should be expected for different metals on a given semi-conductor [8]. However, this does not happen in practice, for a large range of metals on the most common semiconductors, such as, Si, GaAs, InP [9], or CdTe [10]. Other factors that are important in describing Schottky junctions are the depletion layer width (W_o) and the diode ideality factor (n).

Table VII.I .. A summary of measured Schottky barrier heights of metal contacts on p-type CdTe. Semiconductor surface preparation method and barrier detection mode are both indicated.

Metal	Surf.prep. method	ϕ_B	Detec. mode	Ref
Au	air cleaved Br-MeOH etch	1.0 1.1 1.0 1.1	photo C-V Photo C-V	4
Au	vac.cleaved air cleaved	0.5 0.6 0.6	Photo Photo Photo	5
Au	vac.cleaved Br-MeOH etch	0.63 0.59	I-V I-V	6
Au	Br-MeOH etch	0.64 0.6	Photo I-V	16
Al	air cleaved	0.95	I-V	7
Al	vac.cleaved Br-MeOH etch	1.0 0.62	I-V I-V	6
Al	Br-MeOH etch	0.7 0.74	Photo I-V	16
Al	Chem.etch.	0.73	I-V	17

A summary of published data on barrier heights in p-CdTe Schottky diodes is provided in tables VII.I and VII.II. As is evident from both tables, large discrepancies exist between different authors. These inconsistencies can often be attributed to the way in which the semiconductor surface was prepared and/or to the mode of detection. The limitations imposed on the calculated barrier height by the detection mode is touched on in chapter 5. As for the effects of surface preparation, J. G. Werthen et al [6] using X-ray photoelectron analysis indicated

that four different surface compositions result for CdTe single crystals from five different treatments: cleaving (stoichiometric), bromine-in-methanol etch (Te-rich), chromate etch (Te-rich and TeO_2), oxidation in air (TeO_2), hydrogen heat treatment of etched surface (stoichiometric) [6]. Each of these surfaces might be expected to give a different value for the barrier height.

Even though the work function of Au is 1.0 eV larger than that of In, there is little difference in the barrier heights observed between the two metals and p-CdTe. Some workers [12] have associated this with states at the interface which pin the Fermi level close to the centre of the band gap. Courreges et al [15], concluded that an approximation to a normal Schottky barrier can be achieved by vacuum evaporation of indium onto a Br-MeOH etched CdTe surface. However, they found that evaporated In on a sputter-etched surface or sputtered In on a Br-MeOH etched surface, led to an ohmic indium contact suggesting that the surface had been type converted and was effectively the n-type limb of a p-n homojunction as a result of the sputtering

Table VII.II .. Barrier heights of metal contacts on p-type CdTe, (a continuation of table I).

Metal	Surf.prep. method	ϕ_B	Detec. mode	Ref
Cr	vac.cleaved Br-MeOHetch	0.87 0.99 0.65	I-V C-V I-V	6
Cr	Br-MeOHetch	0.65	I-V	14
In	vac.cleaved	1.1	I-V	6
In	Br-MeOHetch	0.84 1.04	C-V	15
In	Br-MeOHetch	0.7 0.73	Photo I-V	16
Ag	Br-MeOHetch	0.73 0.71	Photo I-V	16
Ag	Chem.etch.	0.73	I-V	17
Ni	Br-MeOHetch	0.65 0.66	Photo I-V	16
Sb	Br-MeOHetch	0.7 0.6	Photo I-V	16
Pd	Br-MeOHetch	0.61 0.52	Photo I-V	16
Bi	Br-MeOHetch	0.62 0.66	Photo I-V	16
Cu	Br-MeOHetch	0.65 0.59	Photo I-V	16
Fe	Br-MeOHetch	0.68 0.73	Photo I-V	16
Mg	Chem.etch.	0.73	I-V	17

process. Inconsistent results may also be attributed to a non abrupt junction formation, where gold telluride has been observed on CdTe regardless of the method used to deposit the gold [11]. Defects at the interface are well-known to influence ϕ_B [12]. Of particular interest is the fact that Schottky barriers formed by some metals on CdTe are drastically influenced by oxide layers whereas others are not, for example, on n-CdTe, Ag is significantly influenced by oxide layers and Mn is not. Microscopic observations indicated that these differences are associated with a strong reduction of the oxide by some metals but not by others [13].

Surprisingly none of the papers reviewed gives a value for the ideality factor (n)of the resulting diodes. In general, improvements in the ideality factor have been found to result from successive etching treatments an observation which is attributed to the removal of surface states [19].

7.3. In/CdTe diode preparation

Substrates of {111} CdTe were obtained by orienting, slicing and dicing single crystals into 5 x 5 x 1.6 mm^3 dice from undoped CdTe boules grown in-house by a vapour phase method (see chapter 4). These dice were lapped, cleaned, and chemically etched in a 2% by-volume solution of bromine in methanol, rinsed in methanol and blown dry in a stream of nitrogen. The dice were subsequently doped with phosphorous using the PGD method as outlined in chapter 4. The properties of the substrates have been described in chapter 6. After doping the dice were then polished and chemically etched as before; the Br-MeOH etch was carried out by a pad polish method. Ohmic back contacts were fabricated either with Au or by inducing a p^+ layer of P underneath the gold. The back contacts were then covered with lacomit varnish to protect them from the clearly defined fast chemical etch (Br-MeOH) used to produce a fresh surface of

the CdTe to receive the Schottky contact. Subsequently, an area of indium was deposited by vacuum evaporation in a pressure of 0.6 x 10^{-4} mbar. Each device was then mounted on a clean Cu plate using silver paste to ensure safe handling. Silver paste was also used to apply Cu leads to the indium. After this, devices were ready for characterisation.

7.4. In/CdTe diode characteristics

In/CdTe:P junctions were characterised using current-voltage and capacitance-voltage measurements. Both analysis techniques were carried out in complete darkness and at several temperatures from liquid nitrogen temperature up to 400°C in 25°C steps. As mentioned before; two main intentions lay behind the fabrication of the diode; to test the reliability of the PGD type conversion process and to use the diode characteristics to provide more information about bulk CdTe:P properties.

With regard to the first point comparable results to those previously published for CdTe:P based Schottky diodes should provide sufficient evidence of the efficiency of our type conversion process. As for the second, In/CdTe:P structures were used to demonstrate the effect on diode performance of non-ohmic back contacts to single crystal CdTe:P. Diodes were also useful in determining the profile of net charge carriers throughout the treated dice (see chapter 6).

7.4.1. Diode performance

In/CdTe devices make good Schottky diodes. Figure 7.1(a,b) shows an I-V characteristic of a typical In/CdTe:P diode. At 300°C, this diode had a rectification value of 240 at one volt, and a very low reverse saturation current I_o of 4.1 x 10^{-8} A. Diode ideality factors have not hitherto been reported for such

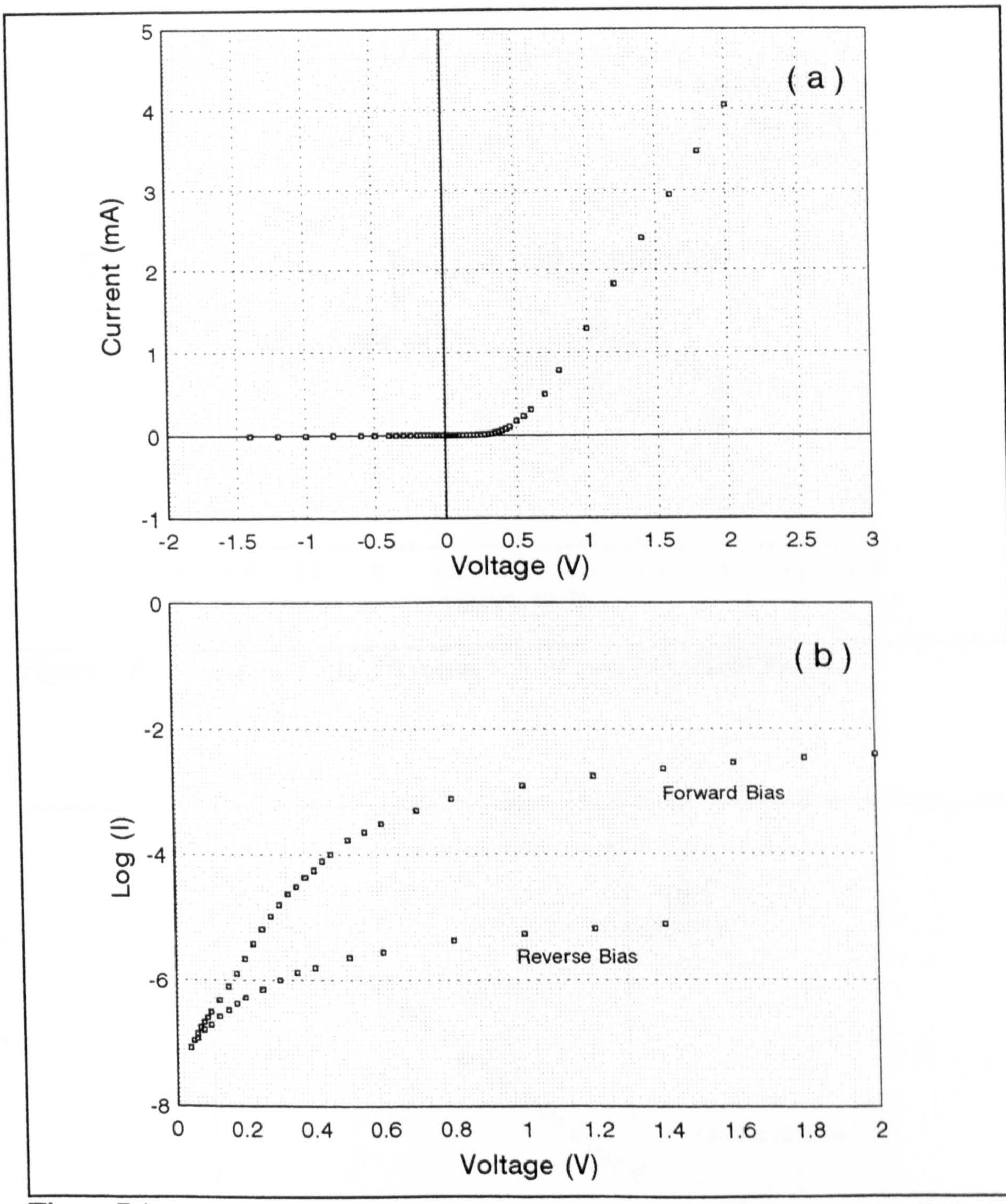

Figure 7.1 .. Room temperature I-V plots of a typical In/CdTe Schottky diode; (a) normal and (b) logarithmic I-V characteristic.

devices, perhaps because of their alarmingly high values; a consequence, possibly, of interface states and oxide layers at the metal/semiconductor interface. This was also the case for one of our diodes, but others, like the one shown in figure 7.1, had an ideality factor (n) of 1.88. This suggests that a recombination carrier

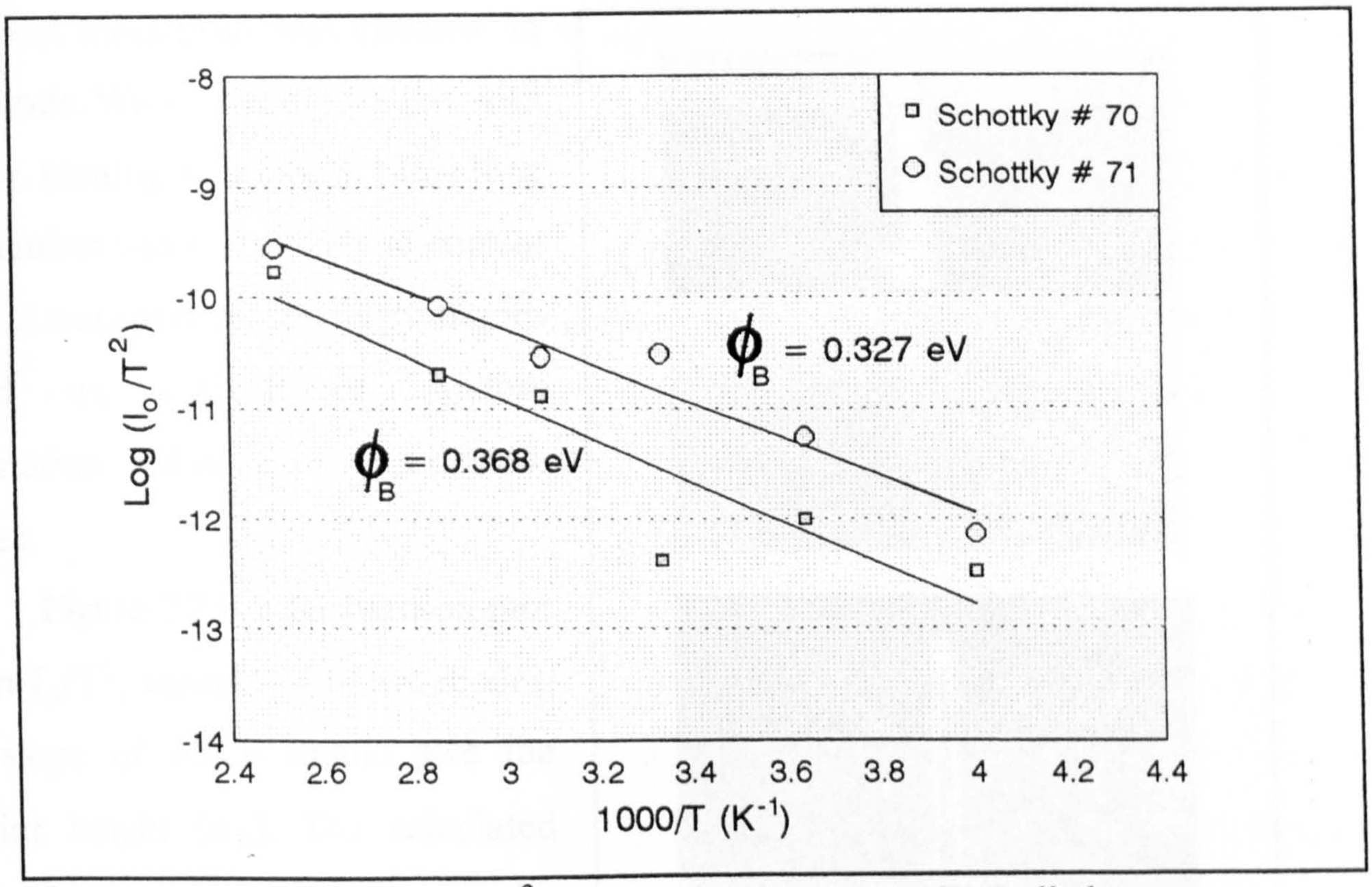

Figure 7.2 .. A plot of $Ln(I_o/T^2)$ versus 1/T of two In/CdTe:P diodes.

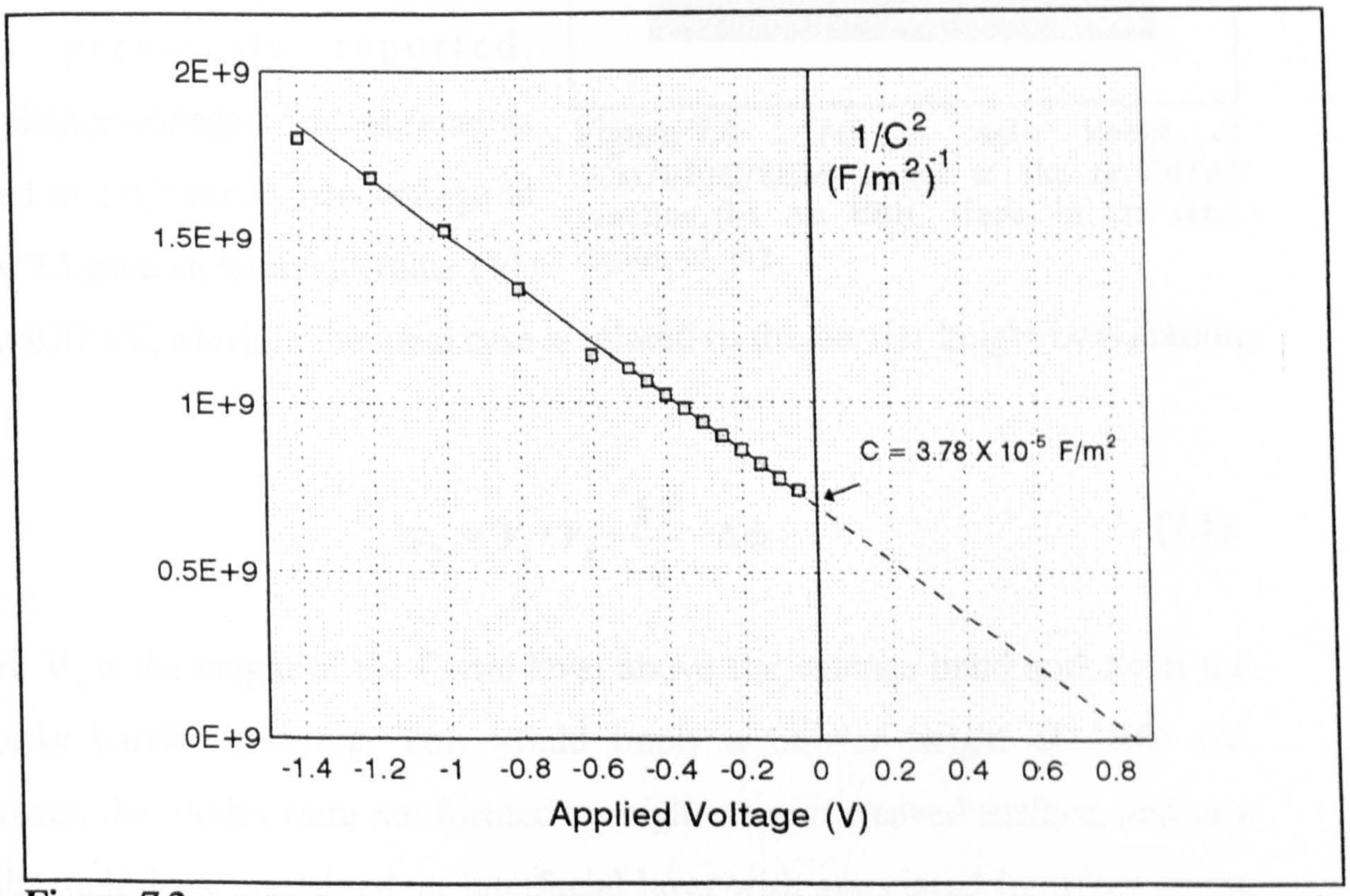

Figure 7.3 .. C-V characteristic of the same In/CdTe:P Schottky diode that is shown in figure 1.

transport mechanism was effective in this diode. With other diodes (i.e. with higher ideality factors), a tunnelling mechanism was more likely to control current transport. Interestingly, diodes based on CdTe:P of random orientation, did not give reproducible values.

Figure 7.2 is a Richardson plot of $Ln(I_o/T^2)$ versus $1/T$ of two diodes, the slope of which should give the barrier height (ϕ_B). The calculated barrier heights for the two diodes were 0.368 eV and 0.327 eV. These values are rather lower than what has been previously reported. Capacitance-voltage measurements plotted as $1/C^2$ versus bias voltage in figure 7.3 gave an intercept value (Vi) about 0.87 eV, which in the ideal case is related to the barrier height by equation (7.1);

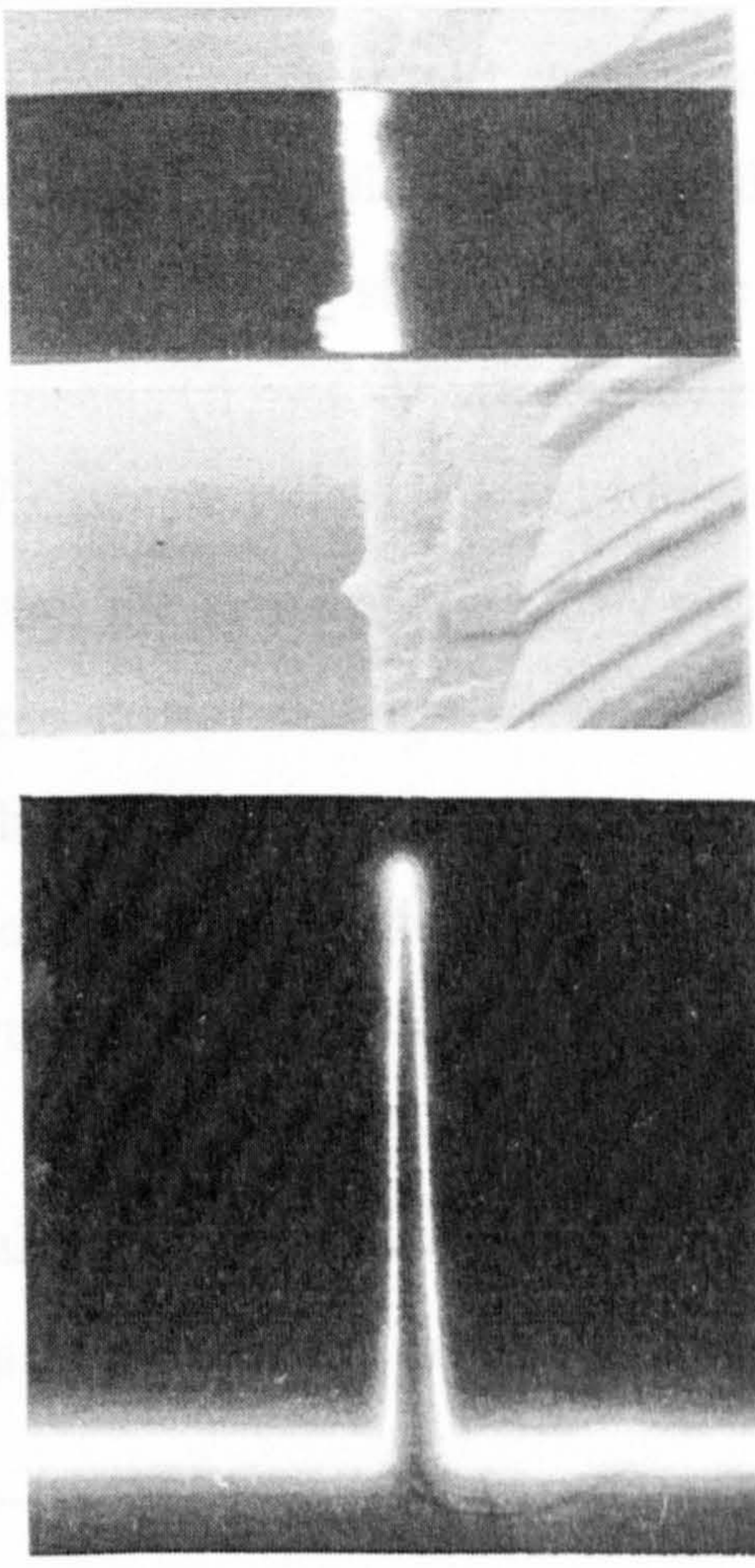

Figure 7.4 .. (a) A split image of SEM/EBIC/SEM image of the In/CdTe:P junction. (b) An EBIC signal in the same region of (a).

$$\phi_B = V_i + V_n + \frac{kT}{q} - \Delta\phi \qquad (7.1)$$

where V_n is the height of the Fermi level above the valence band and $\Delta\phi$ is the Schottky barrier lowering. This would imply a barrier height of ~0.85 eV. However, the diodes were not formed on high vacuum cleaved surface, and as a result would have contained an interfacial layer with associated interface states.

The charge stored in these states would affect the capacitance measurements (since capacitance measurements in reality measure stored charge) and lead to an intercept value different to that predicted by simple theory. The disparity in the I-V and C-V values of the ϕ_B is confirmation that such states were present in the In/CdTe:P diodes. Barrier heights measured by C-V are usually expected to be higher than that measured from I-V characteristics. The net ionised acceptor concentration ($N_a^- - N_d^+$) calculated from the slope of the C^{-2}-V plot was 1.7 x 10^{14} cm^{-3}, somewhat lower than the free carrier density determined from Hall measurements (8.85 x 10^{14} cm^{-3}, for the same dice), but of the same order of magnitude. Both Hall and C-V measurements were useful in optimising the PGD doping techniques, the latter were particularly useful in determining the doping profiles of our dice in the initial doping experiments, (see chapter 6). Occasionally, in the initial doping trials resultant C^{-2}-V plots were not straight lines, indicating a non uniform distribution of carriers in the depletion region or

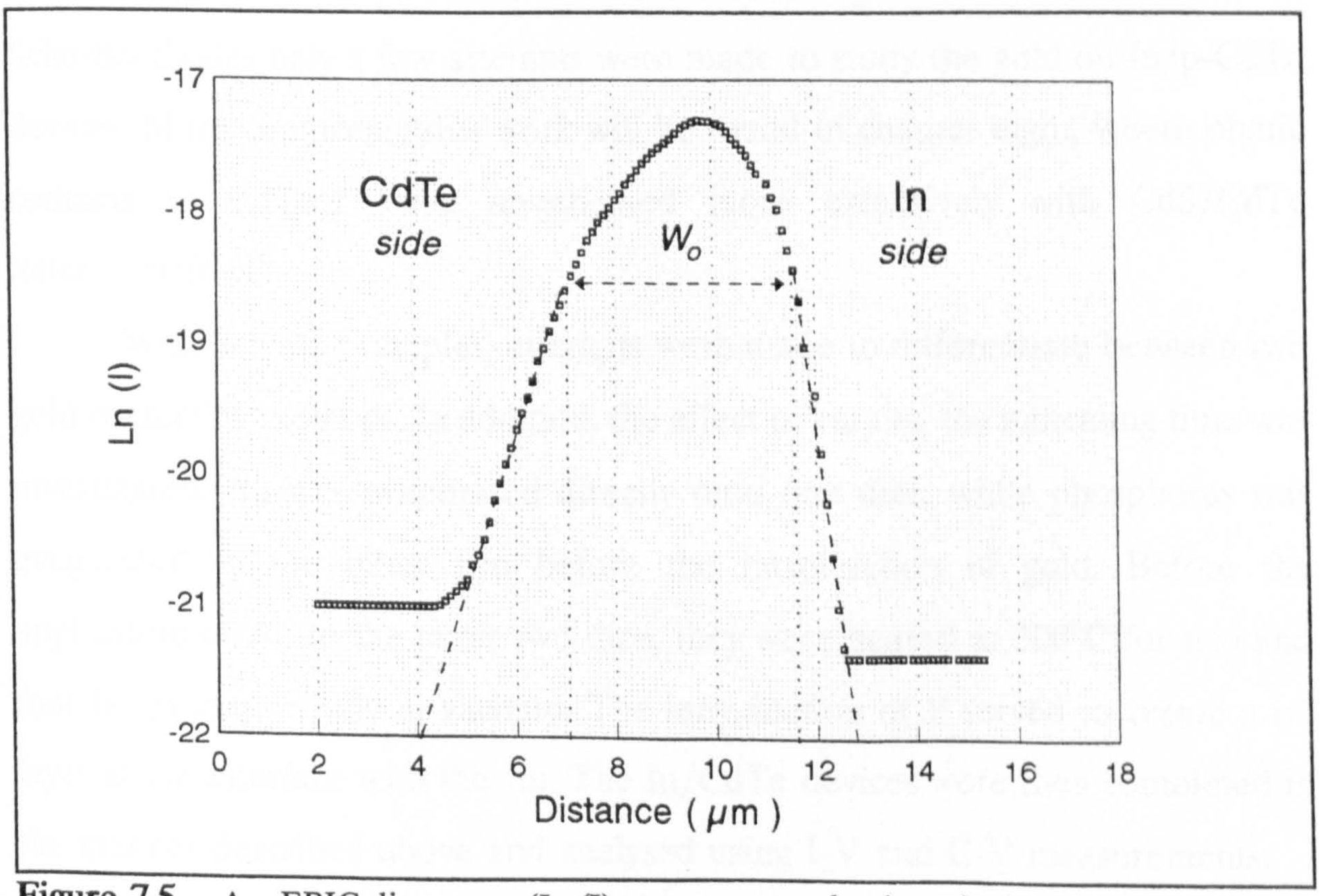

Figure 7.5 .. An EBIC line scan (Ln(I) vs x across the junction) of the diode shown in figure 4.

bias dependent interface states. From figure 7.3, the calculated depletion region width (W_o) was 2.4 x 10^{-6} m.

This diode was, also, subjected to EBIC examinations in the SEM. Figure 7.4 gives split SEM and EBIC images of a vertical cross section of the junction. The higher contrast region in the EBIC image lies on the CdTe side as expected, since it should lie in the less conductive material. Figure 7.4 also shows the EBIC signal of the diode, it clearly lies within the depletion region. EBIC measurements are useful in determining the minority carrier diffusion length (L) and the depletion width (W_o). A measured EBIC line scan of the diode is shown in Figure 7.5. The L and W_o were measured to be 0.908 μm and 4.1μm, respectively.

7.4.2. Back contacts to In/CdTe:P

The fabrication of an ohmic contact to p-CdTe is known to be a considerable problem with CdTe devices. Gold was used for a time but proved to be a highly resistive contact due to a rather high barrier. In the work on Schottky diodes only a few attempts were made to study the gold on In/p-CdTe devices. More comprehensive work will be found in chapter eight, where ohmic contacts to CdTe:P were investigated more extensively with CdS/CdTe heterojunctions.

With Schottky samples, attempts were made to differentiate between two gold contacting methods. In addition, the effect of varying the annealing time was investigated. Au was evaporated directly onto one dice, while phosphorus was evaporated to the other two before the introduction of gold. Before the application of Au to the latter two dice, they were heated at 300°C for two and four hours respectively in vacuum. The introduction of P served to create a p^+ layer at the interface with the Au. The In/CdTe devices were then completed in the manner described above and analysed using I-V and C-V measurements.

Two sets of results may be obtained from these trials. The first set

comprised the Au (no phosphorus) and the P (2 hour annealed)-Au back contacted diodes and their I-V characteristics are shown in figure 7.6. The device with the direct gold contact gave a characteristic that is similar to a back-to-back Schottky diode, where it appears that In and Au are both forming barriers with the semiconductor. This implication was supported by the C-V test, where the slope of the curve changed from positive to negative after few millivolts. A much

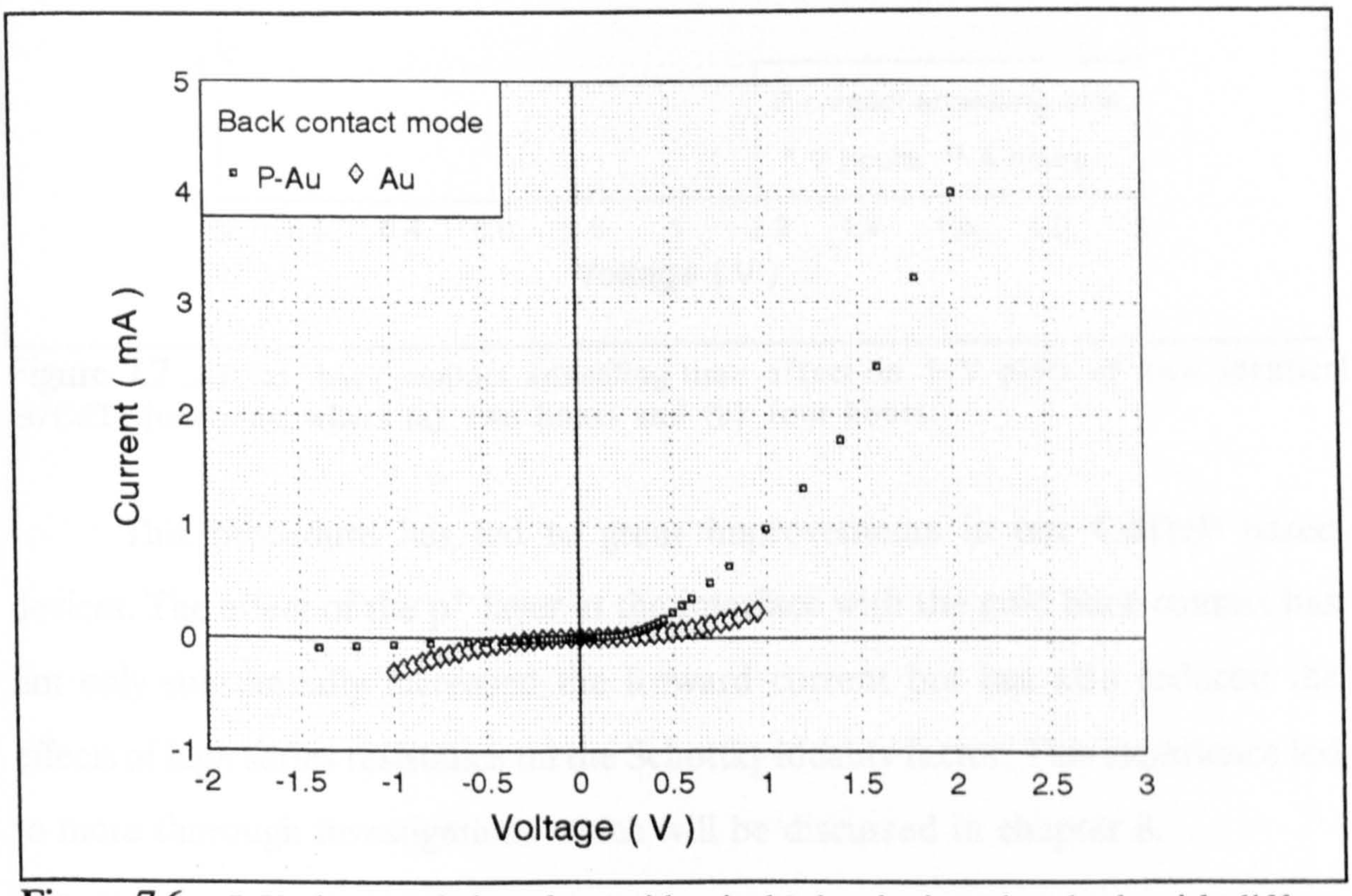

Figure 7.6 .. I-V characteristics of two identical Schottky junctions both with different back contacts; where (a) P (2 hours anneal) + Au and (b) Au only.

improved performance was obtained with the p^+(2 hours anneal)-Au contacted diode, see figure 7.6. The effect of changing the annealing time of the phosphorus treated contacts from two to four hours is illustrated in figure 7.7. It is clear that the characteristics of the 4 hour annealed diode followed the usual logarithmic I-V equation for Schottky diodes, more closely, up to a bias voltage of ˜0.5 V, where series resistance effects became dominant.

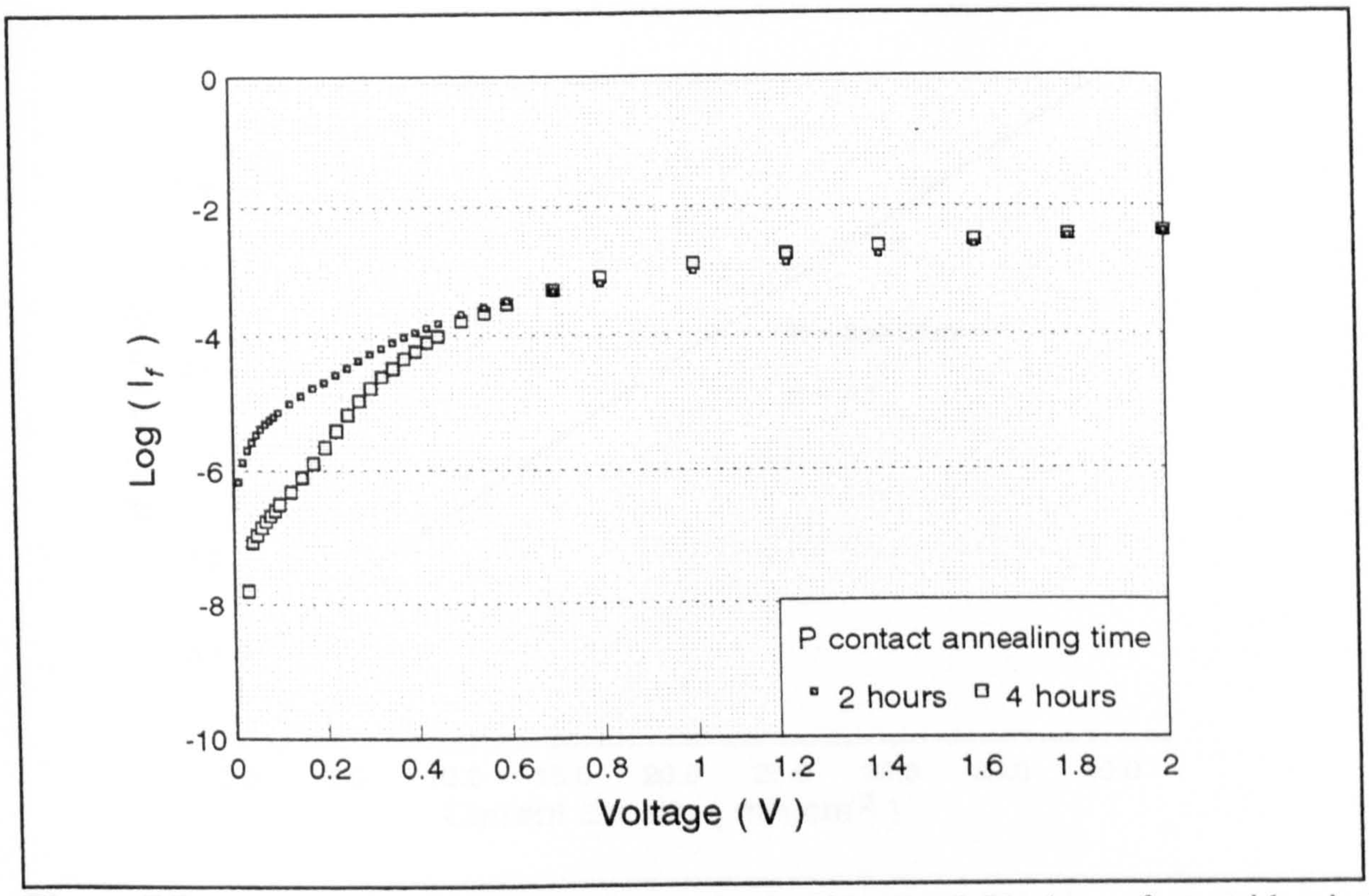

Figure 7.7 .. P as back contact annealing time effect on I-V plots of two identical In/CdTe junctions; where (a) two hours and (b) four hours.

This procedure has led to great improvements in our CdTe:P based devices. The effect of the p^+ layer at the interface with the gold back contact has not only substantially increased the forward current but has also reduced the effects of high series resistance on the Schottky ideality factor. This experience led to more thorough investigations which will be discussed in chapter 8.

7.5. Discussion and Conclusion

A method of extracting Schottky diode parameters from forward current-voltage characteristics, was introduced by Cheung and Cheung [18], for deducing device series resistance, is outlined in chapter 2 (along with others). The relevant features are that a plot of d(V)/d(lnJ) versus J gives $R_s A_{eff}$ (where A_{eff}; junction effective area) from the slope and nkT/q from the y-axis intercept. Figures 7.8

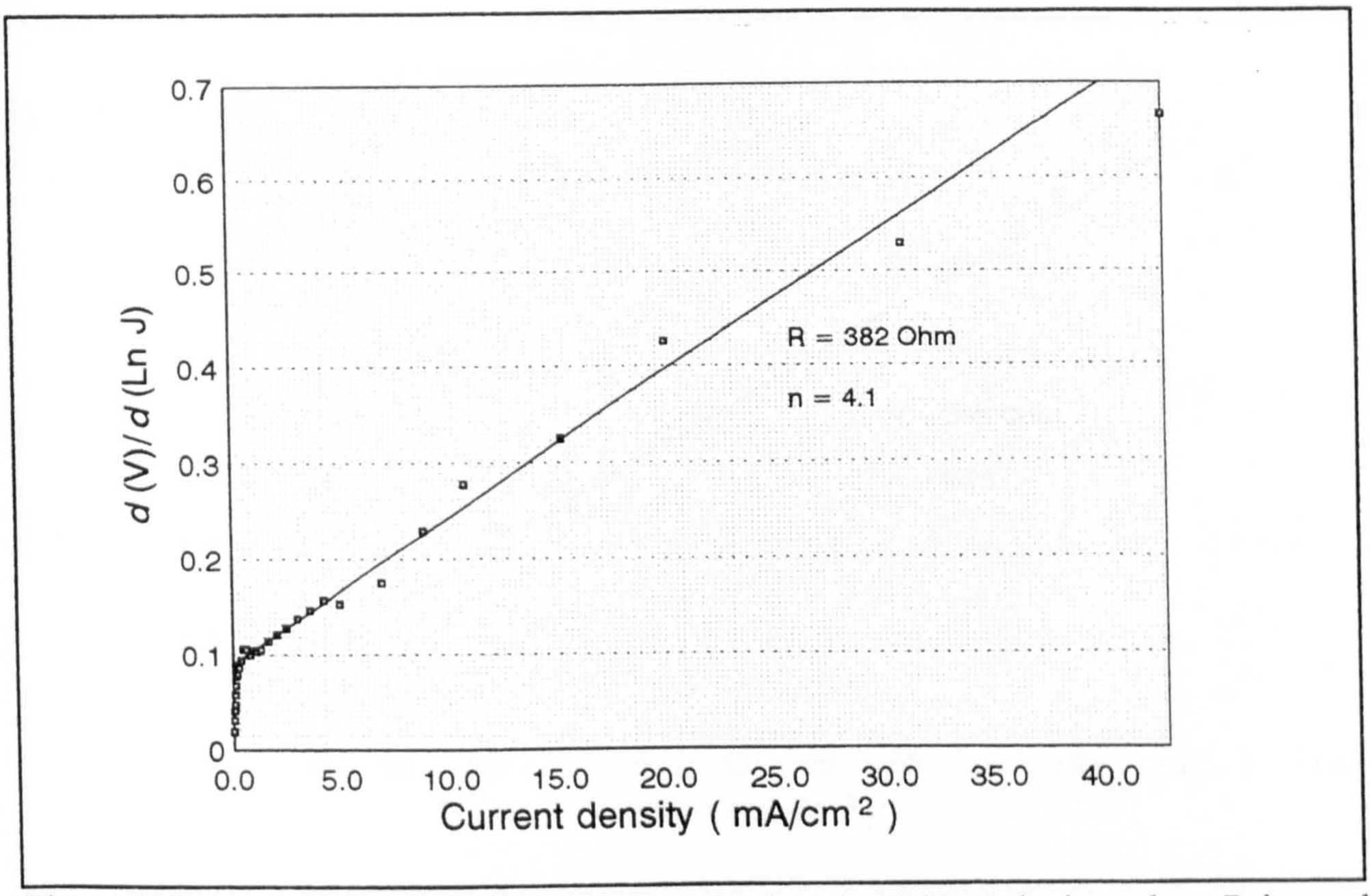

Figure 7.8 .. A plot of d(V)/d(Ln(J)) versus J of an In/CdTe:P device, where P is used in the back contact formation and subjected to a two hour anneal.

and 7.9 show such plots for the two and four hour annealed devices, respectively. The ideality factors determined from this method were slightly larger than those derived from temperature dependent I-V's; i.e. 4.1 and 2.08 whereas both devices gave n= 2 from I-V characteristics. The calculated series resistances for the two and four hour annealed devices were 382Ω and 338Ω. A similar analysis for the directly contacted device (i.e. no P treatment) gave a value of 835Ω for the series resistance. These results clearly demonstrate the contribution of the back contact to the overall resistance of Schottky devices, and help explain the poorer performance of the directly contacted device. The decrease in the series resistance for the p^+ layered devices results from the high doping of the semiconductor near the Au/CdTe:P junction, which allows current to be carried by tunneling through the barrier. (At the same time the bulk CdTe:P may be additionally doped with P by allowing more time for the introduced P to diffuse into the semiconductor).

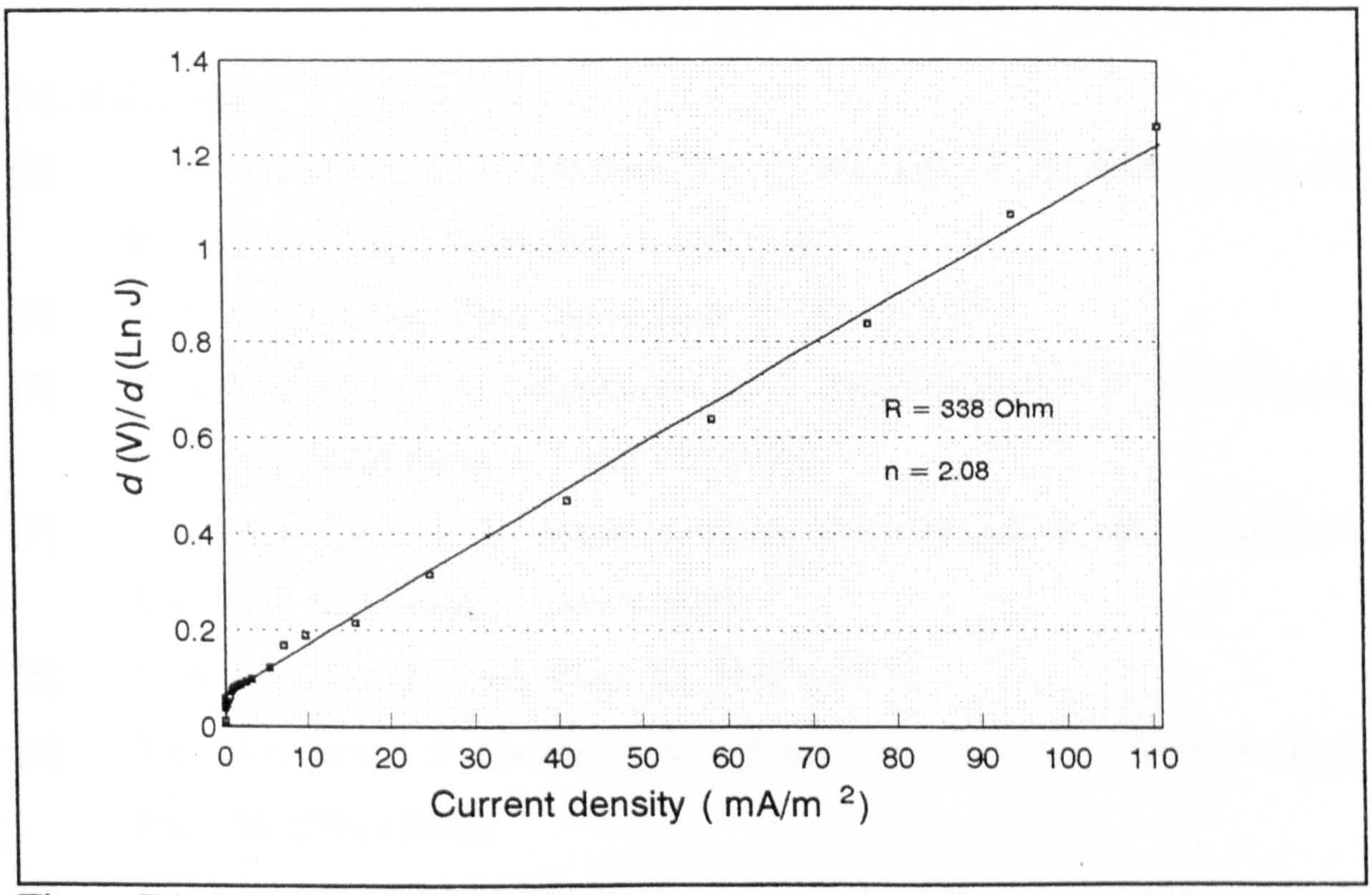

Figure 7.9 .. A plot of d(V)/d(Ln(J) versus J of an In/CdTe:P device, where P is used in the back contact formation and subjected to a four hour anneal.

The CdTe semiconductor surface clearly plays an important role in the behaviour of subsequently formed junctions, with the surface preparation method probably governing the interface properties in the metal/p-CdTe junctions.

In summary, the PGD process for the phosphorus doping of CdTe has clearly been effective in influencing the semiconductor type conversion. Rectifying contacts were formed by depositing an electropositive metal (In) onto the CdTe:P surface. In/CdTe junctions have been characterised using I-V, C-V and EBIC measurements. In spite of the low measured barrier height, diodes showed obvious Schottky junction behaviour. Thus considerable progress has been made in solving the problems of bulk resistivity and ohmic back contacts in p-CdTe based junctions. The problem of back contacts in solar cells will be taken up in the next chapter, where ohmic contacts to CdTe:P in CdS/CdTe structures is the main issue.

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Chapter VIII

Ohmic Contacts to CdTe:P

8.1. Preface

One of the outstanding problems to be overcome before efficient, heterojunction PV cells based on p-type CdTe can be produced successfully, lies in the difficulty of preparing a good ohmic contact to the CdTe. The problem obviously becomes more apparent as the technology of producing low resistivity p-type CdTe improves. Thus having developed the doping of p-type CdTe, as described in a preceding chapter, attention was focussed on the fabrication of an ohmic contact. Before discussing the present research, a brief review of published data will be given.

8.2. Ohmic contacts to p-CdTe

8.2.1. Approaches

In the investigation of the electrical properties of semiconductor devices, the nature of any semiconductor to metal connection is extremely important. Usually, it is desired that such a contact be ohmic. In practice, a contact is considered ohmic if the voltage drop across it with either polarity is much smaller than that across the device, and hence does not perturb significantly the device characteristics. There are three major approaches to achieving an ohmic contact:

1) by choosing a metal with the proper relative Fermi level so that the barrier is small for thermally excited current carriers.

2) by heavily doping the semiconductor near the junction so that the current can be carried by quantum mechanical tunneling through the barrier.

3) by introducing numerous recombination centres in the interface region on the semiconductor side of the junction to promote multistep tunnelling.

Since CdTe has a high value of electronegativity and electron affinity, there is no metal with a high enough work function to provide a low resistance ohmic contact by approach (1) above. This is further aggravated by effects caused by surface states and interfacial layers. Thus barrier height engineering (first approach) is not a realistic way of making ohmic contacts to p-CdTe. The use of conventional metals and damaged surfaces to create high densities of generation-recombination centres at the interface (third approach) is not a good reproducible technique either, because such damage-generated centres can penetrate some distance into the semiconductor and may cause other problems, especially in thin active layers. This leaves as the only practical technique, the second approach, in which the metal is deposited onto a highly doped semiconductor.

Although the barrier height ϕ_B is not dependent on the doping density, the electrostatic attraction of the charge carriers in the semiconductor towards the metal surface by an induced mirror charge of opposite sign in the metal, has the effect of lowering the barrier by [1]

$$\Delta\phi = \left[\frac{q^2 E_b N_A^-}{8\pi^2 \epsilon_s \epsilon_d^2 \epsilon_0^3}\right]^{1/4} \qquad (8.1)$$

The depletion layer width W, which is the space charge region in the semiconductor adjacent to the metal layer, is related to the ionised acceptor concentration N^-_A by [2]

$$W = \left[\frac{2E_b \epsilon_s \epsilon_0}{q^2 N_A^-}\right]^{1/2} \qquad (8.2)$$

Where, E_b is the energy band bending in the semiconductor depletion region, ε_s the static dielectric constant, ε_0 the permittivity of free space, and ε_d the relative

dynamic (high frequency) dielectric constant of the semiconductor. As the acceptor concentration is increased, barrier narrowing ($W \alpha N^-_A{}^{-\frac{1}{2}}$) proceeds more rapidly than barrier lowering ($\Delta\phi \alpha N^-_A{}^{1/4}$), and, consequently, as doping is increased, conduction becomes dominated by quantum-mechanical tunneling through a narrowed barrier rather than by thermionic emission over a lowered barrier. Ponpon [3] predicted that carrier densities p of about 3×10^{18} cm^{-3} for $\phi_b = 0.6$ eV and p of about $7x10^{17}$ cm^{-3} for $\phi_b = 0.5$ eV would be required to make $\rho_c < 0.2$ Ωcm^2, which was calculated by Fahrenbruch [4] to be an optimum specific contact resistivity for CdTe based solar cells.

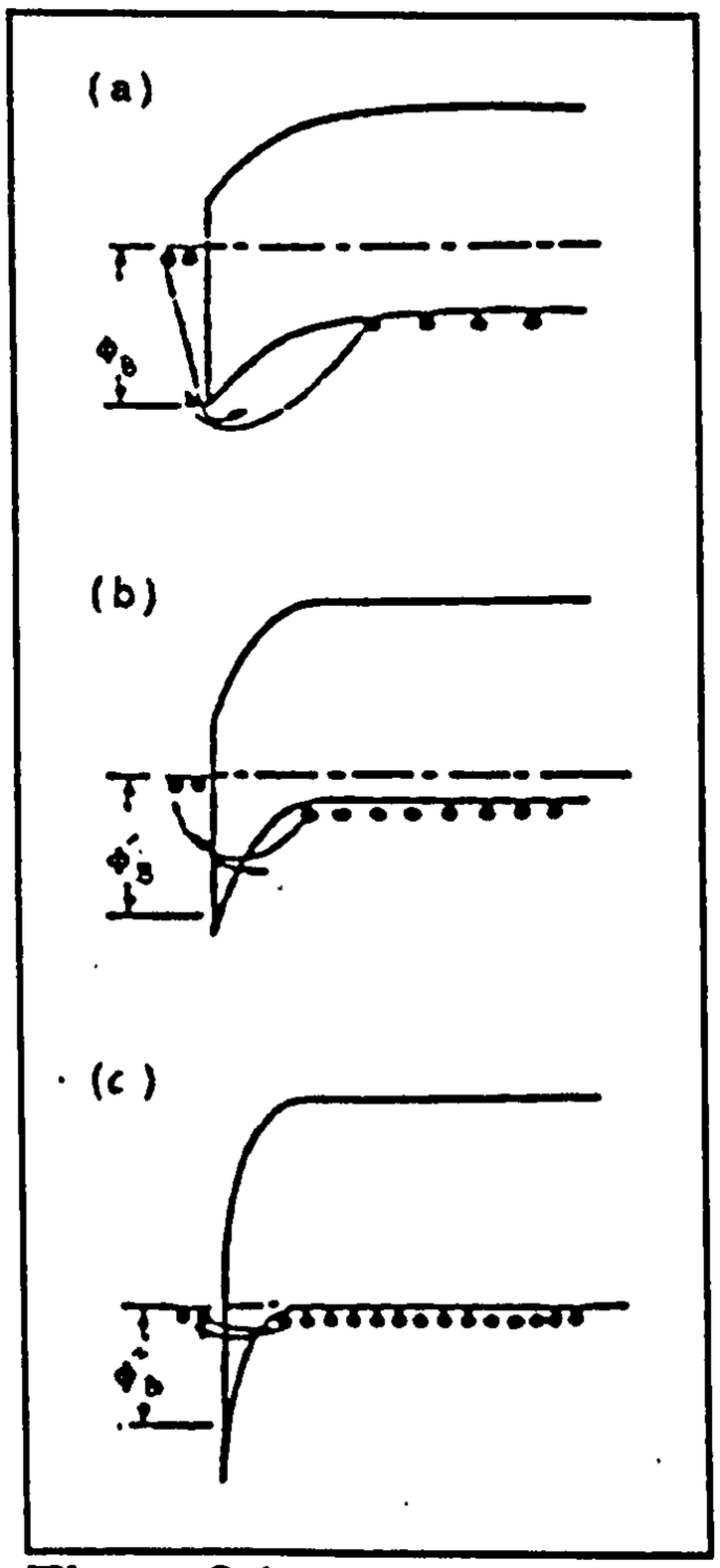

Figure 8.1 .. Barrier height and width and conduction mechanism for metal/p-semiconductor contacts with increasing semiconductor dopant concentration.

Potential energy diagrams for metal/p-semiconductor contacts with increasing dopant concentration are shown in figure 8.1 and 8.2. For low doped substrates, the current is the result of thermionic emission over the barrier shown in figure 8.1a. For high doping levels, shown in figure 8.1c, the barrier is thin enough at or near the top of the valence band that tunneling is the dominant mechanism (see figure 8.2). Obviously in intermediate ranges, a combination of both mechanisms is dominant, when the carriers are excited thermally to an energy less than the full barrier height. At this

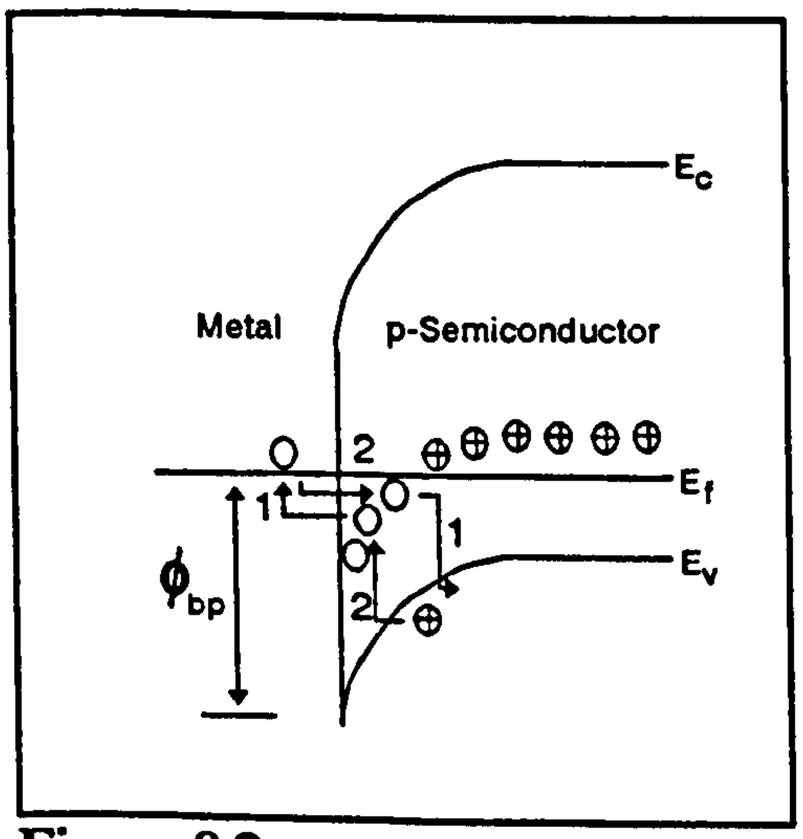

Figure 8.2 .. Trap-assistedtunneling process for Schottky barrier (step sequence is as indicated.

energy the barrier is sufficiently thin for tunneling to take place.

Hence, a likely solution for the production of ohmic contacts to p-CdTe would be to place a layer of gold in contact with a heavily doped p-type region of the semiconductor. The objective is to achieve field-emission-dominated conduction so that the potential barrier will appear to be almost transparent to carrier flow.

8.2.2. Ohmic contacts to p-CdTe

The aim of this section is to review the previous experimental work on ohmic contacts to p-type single crystal CdTe. In general, the formation of an ohmic contact on cadmium telluride is difficult, espẽcially on p-type material, because of (1) the low doping efficiency of most of the impurities that can be introduced, (2) the presence of a high resistance surface layer, and most significantly, the high value, 5.9 eV, of the electron affinity of the material. A distinct difference between the analytical approach used here and other studies of ohmic contacts is their use of the specific contact resistance ρ_c (Ω cm^2) as a measure of performance, while in this chapter it has not proved possible to measure ρ_c, so that the influence of different contacts on device characterisation has been investigated instead. Nevertheless, it is worthwhile to review published results to highlight particular trends.

To overcome the problem of high CdTe electron affinity, some research has alternatively used compound materials of higher work function. A variation of this theme is to interpose between the CdTe and the metal a layer of another semiconductor which forms an ohmic contact to the metal more easily and that has suitable electron affinity match with p-CdTe. E.Janik et al [5] used a high-work-function-compound (HgTe, 5.9 eV), which was deposited by vapour-phase epitaxy on bromine-in-methanol etched p-CdTe of 10-15 Ωcm resistivity ($N_A \approx 8x10^{15}$ cm^{-3}), this approach gave a non-rectifying junction down to 20K. An

alternative possibility is the use of a high conductivity p-type buffer layer, such as ZnTe or CdHgTe between the CdTe and the metal contact [6].

As for the contact metals, the work functions of Cu, Au, Ag, Zn, In and Pb on p-CdTe have been determined and Au has been found to be the most favorable [7], so the most widely used and researched contact to p-CdTe is gold [4]. It may be used alone or as a final metal layer, applied after various surface treatments. One such method of forming a gold contact is by vapour deposition of gold or Au-Cu alloy onto a surface, previously etched with certain solutions such as H_2SO_4-$K_2Cr_2O_7$-H_2O ("B" etch), HNO_3-HCl-H_2O [8], or Br_2-MeOH [9]. Although, the "B" etch has been reported [10] to provide a ρ_c value 10-60 times lower than that obtainable with Br_2-MeOH, interestingly, in conjunction with a photovoltaic barrier, it yields a high value of J_o (low V_{oc}), whereas a bromine-methanol etch leads to a much higher V_{oc}.

One of the first methods used to produce ohmic contacts on p-CdTe was electrolysis deposition of a noble metal from solution, generally the chloride. In this way contacts of Ag, Au, Ir, Pt and Rh have been obtained [3]. According to De Nobel [11] during the reaction with gold chloride, cadmium would leave the semiconductor to go into the solution as Cd^{++} ions, leaving a p-type tellurium film at the surface with the gold. Structural studies of gold electroless contacts on p-type CdTe [12] have shown more precisely that in addition to the model proposed by De Nobel, gold diffuses into the semiconductor and introduces acceptor sites which are responsible for the increase in the current by tunneling when compared with a simple Au or Te surface barrier. In any case very low ρ_c cannot be achieved by this method owing to the low doping efficiency of gold as an acceptor in CdTe [13]. However, others [14] have tried to achieve the required effect by evaporating gold or platinum and firing at 200°C in a hydrogen atmosphere.

Many other methods have been used with varying degrees of success:

among them one somewhat similar to our approach which is to alloy the acceptor dopants (Cu, Ag, P, Sb, Bi) using tellurium as a solvent [15]. Gold has also been evaporated onto As^+ implanted layers [16]. A laser-induced-diffusion-technique using Au and Cd_3P_2 evaporated films with 1 ms pulses from a krypton laser was preferred by Tews and An [17]. However, Ponpon [3] argued against the use of Li and P, even though they are shallow acceptors, because of their high mobility which it was suggested, would result in precipitation making it difficult to introduce them in concentrations higher than 10^{17}-$10^{18}\,cm^{-3}$.Other acceptors such as Au and Cu, have rather higher ionisation energies (0.3-0.4 eV) and in high concentration they can behave as interstitial donors. In spite of that, it was suggested that copper would give the best results if it was introduced at a level of $10^{18}\ cm^{-3}$ [18] (which is possible), whereas gold cannot give active acceptors densities in excess of 10^{16}-$10^{17}\,cm^{-3}$ [13].

A number of methods for introducing the dopants at the required densities involve novel processes. Much interest has been shown recently in laser annealing, as it may offer interesting opportunities to introduce dopants in excess of the

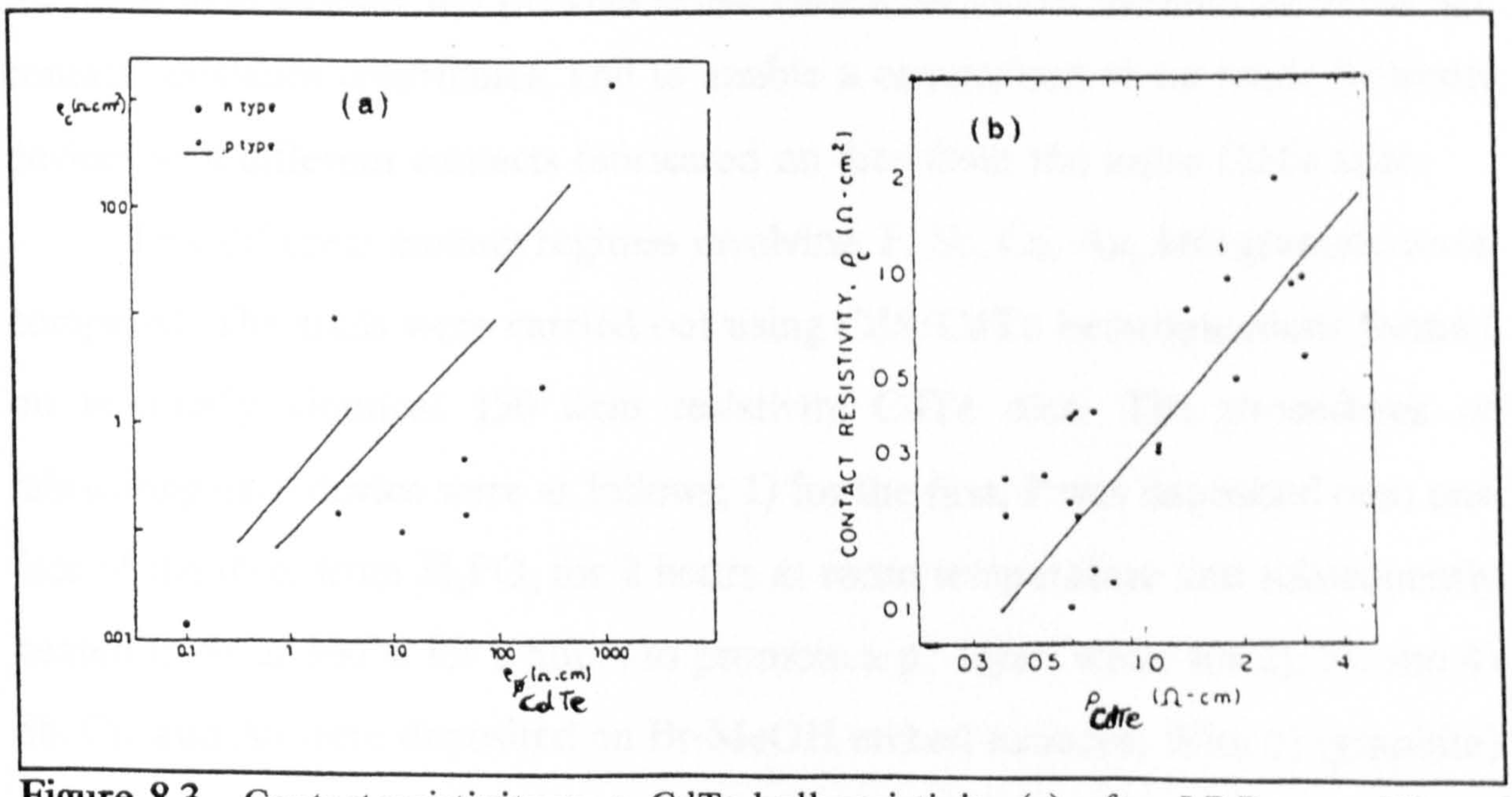

Figure 8.3 .. Contact resistivity vs. p-CdTe bulk resistivity.(a) after J.P.Ponpon [3], and (b) after T.C.Anthony [10]; for an Au-Cu contact.

solubility limit thus leading to improvements in the realisation of ohmic contacts. An and co-workers [17] used laser annealing of $Au/Cd_3P_2/CdTe$ and Au/CdTe contacts.

The evolution of contact resistivity with CdTe bulk resistivity is shown in figure 8.3(a,b). A rough linear dependence of ρ_c on ρ is observed. The final conclusion to be drawn is that the formation of a low specific resistance contact on p-type cadmium telluride implies either the use of very high (p-type) work function material or the introduction of a large concentration of acceptors into the semiconductor in order to increase the current flow by tunnelling.

8.3. Experimental Procedure

In an attempt to study the effect of back contacts on solar cell performance, several modifications were made to the solar simulator; AM1 test conditions were established, together with continuous monitoring of the illumination intensity, and active control of the device temperature; details are given in chapter 5 section 5.5.4. A method, outlined in chapter 2 section 2.4.2.1.1., was used to determine the internal series resistance of our devices, to which the contact resistance contributes, and to enable a comparison to be made between devices with different contacts fabricated on dice from the same CdTe slice.

Five different contact regimes involving, P, Sb, Cu, Au, and graphite were compared. The trials were carried out using CdS/CdTe heterojunctions formed on nominally identical 150 Ωcm resistivity CdTe dice. The procedures of fabricating each device were as follows; 1) for the first, P was deposited onto one face of the dice, from H_3PO_4 for 2 hours at room temperature and subsequently heated in Ar at 300°C for 2 hours to promote a p^+ layer; while for 2), 3), and 4) Sb, Cu, and Au were deposited on Br-MeOH etched surfaces; With 5) (graphite) there was no initial back-contact treatment. All five dice were placed in an

evaporation chamber and heated at 220°C for 30 minutes after which CdS was deposited on the other large area face. Graphite was applied to the fifth dice after CdS deposition. All five devices were, then, heated at 200°C for 30 minutes in a nitrogen atmosphere, to anneal the graphite contact and to induce further material diffusion in the other cases. Gold was re-evaporated onto the first four devices, where a p^+ skin should have been formed at the p-CdTe surface. An indium contact was evaporated on the undoped CdS to form the device top contact. Opaque masks were then used to define effective illuminated areas of each device. Cells were now ready for I-V measurements.

8.4. Effect of the Contact Material on the Current-Voltage Characteristics

In the dark and with an external bias supply, the diode I-V characteristic is in principle described by (8.3)

$$I = I_o\left(\exp\left[\frac{q}{nkT}(V-IR_s)\right]-1\right) \tag{8.3}$$

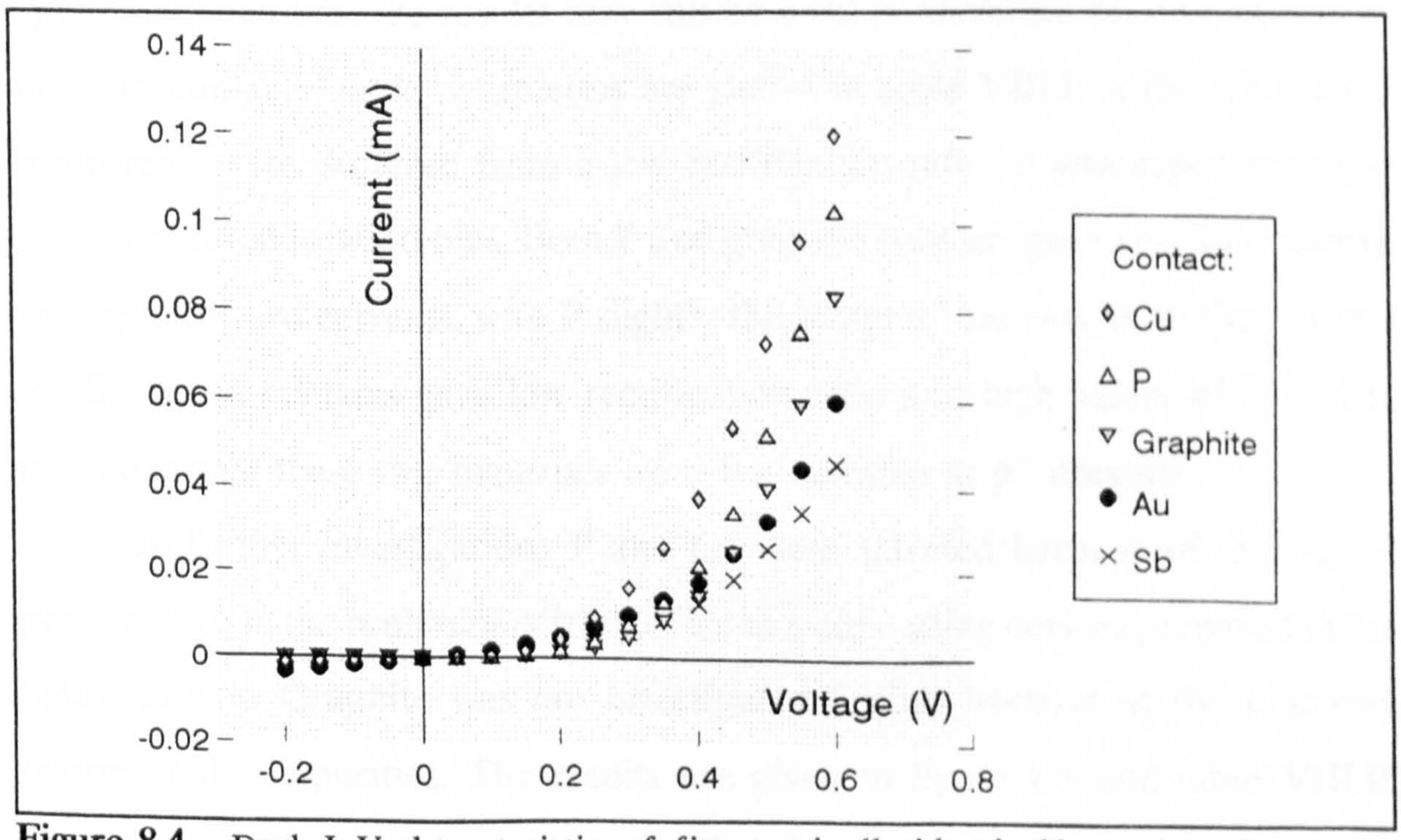

Figure 8.4 .. Dark I-V characteristics of five nominally identical heterojunctions made with different contacting materials to p-CdTe.

where shunt resistance effects have been neglected.

The voltage drop caused by the current flow through the internal series resistance, R_s, affects the diode output current directly. The lower the resistance, the higher the current, and vice versa. Hence junction output currents may be used as a relative indicator of the internal resistances of devices, and since the only difference between our devices were the back contacts, information was provided about the effect of the contacting materials on the I-V characteristics. Figure 8.4 shows the dark I-V characteristics for the five devices. Although these devices were made early in the research under non-optimum conditions, the results may still be used to show the relative effects of the back contact. Diode parameters are shown in table VIII.I. Although the Cu contacted device, suffered from a low rectification ratio, it was superior to the other devices in forward bias. Both P and graphite contacts gave very low reverse and high forward currents, with P slightly the better of the two. Both the Au and the Sb doped contacts gave low rectification ratio and high values of I_o and n, indicating that these two materials were less suitable as p^+ dopants.

Table VIII.I .. Diode factors of five differently contacted CdS/CdTe heterojunctions, (*; junction rectification).

Contact	Rec.*	I_o	n
Au	6.7	$8.3x10^{-7}$	4.2
Cu	18.2	$9.2x10^{-8}$	2
Graphite	166	$8.7x10^{-8}$	2.9
P	104	$1x10^{-7}$	2.4
Sb	15.9	$2.5x10^{-7}$	3.2

In further investigations P and Cu were selected because of their good performance in the preliminary trials. This was done using devices prepared in the optimum way. Graphite was not investigated further because of the unknown nature of the impurities. The results are given in figure 8.5 and table VIII.II. Some modifications to the preparational techniques were employed. Dice onto

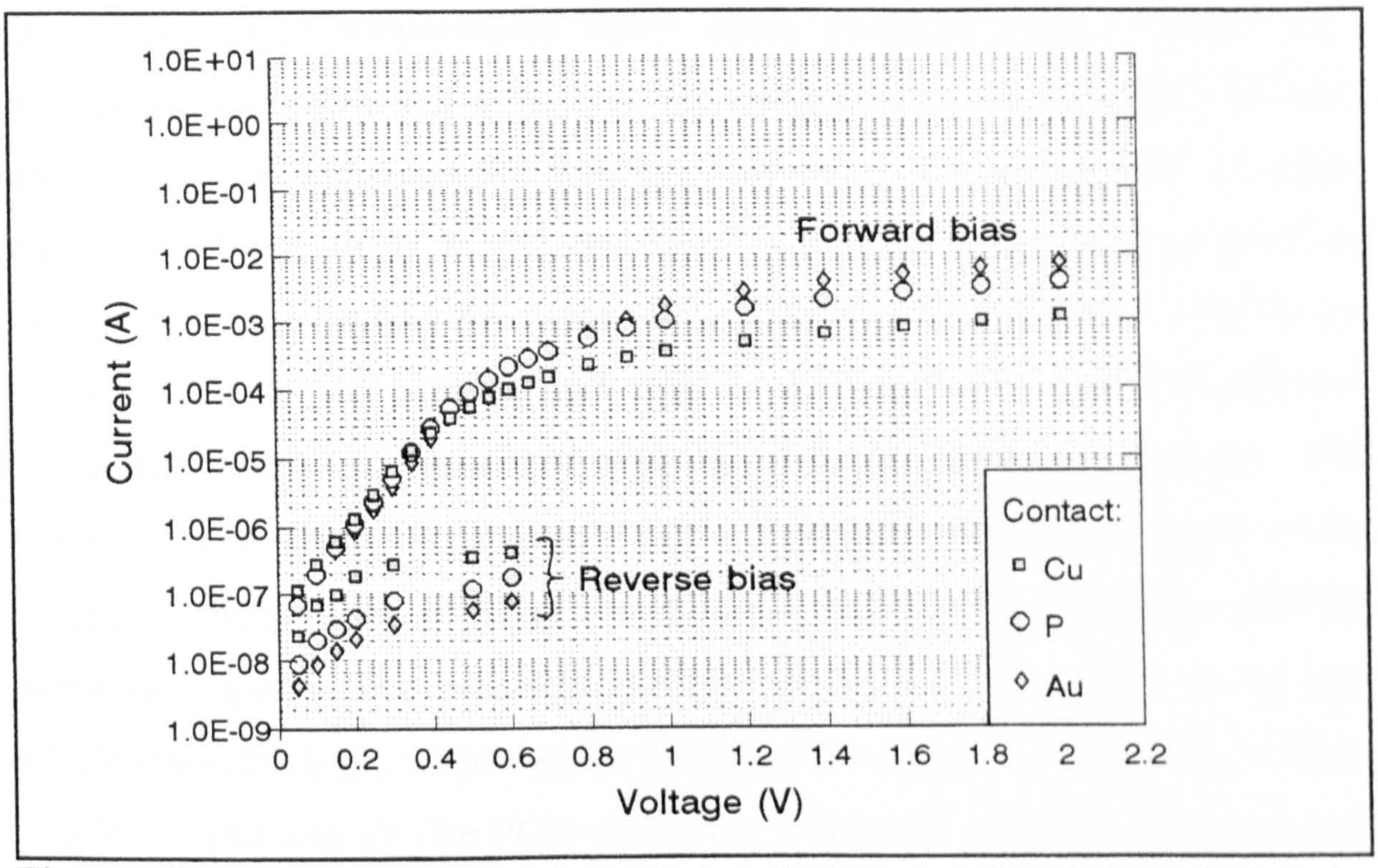

Figure 8.5 .. A logarithmic plot of the dark I-V characteristics of three devices that differ only in the back contact formation.

which P had been deposited were annealed before CdS deposition for 4 rather than only 2 hours, and Au was evaporated onto the CdTe side of the dice after CdS deposition rather than before. In addition no further heat was applied to the devices after heterojunction formation. As expected, at low voltages, where series resistance was not a dominant factor, junction currents were much the same. At higher voltages (V > 0.6 V), the effects of device resistance were more pronounced, and currents differed from one diode to another.

Table VIII.II .. CdS/CdTe heterojunction parameters of three devices differing only by the back contact material.(*; junction rectification).

Contact	I_o	n	Rec.*
Au	$3.4x10^{-8}$	1.63	2727
Cu	$5.6x10^{-8}$	1.09	238
P	$4.1x10^{-8}$	1.29	1167

The three devices were tested at several temperatures, between 77K and 400K in 25K increments although no measurable response was obtained for any

of the devices at temperatures below 130K. Junction ideality factors were maintained reasonably well at low and high temperatures, indicating that the back contacts do not influence the junction behaviour, i.e. the current transport mechanism. Interestingly, for Cu, Au, and P, the first measurable response from the devices to the applied bias at low temperatures was observed at 200K for Cu contacts, 150K for Au contacts, and 130K for P contacts. This was probably due to carrier freeze out associated with the various acceptor impurities. The temperature at which the currents fall below the detection level depends on the acceptor density in the p^+ layer and the activation energy associated with the particular impurity. The ionisation energies for Au and Cu in CdTe are 0.3 and 0.4 eV respectively [3], while that for P is less well known. We have found values of 0.36 eV and 0.46 eV (for PGD CdTe, see chapter 6) although a value of 0.04 has been reported in the literature [19]. The temperatures at which the response fell below the detection levels in our case are commensurate with the activation energies of the three dopants, although the lower temperatures found for the P contacts (as compared to the Au) probably indicate a much higher doping concentration was achieved with P than with Au.

8.5. Effect of Contact Material on Photovoltaic Properties

The series resistance imposes limitations on the maximum attainable efficiency of solar energy conversion. Theoretical plots for combinations of R_s and R_{sh} (series and shunt resistances, respectively) are given in figure 8.6, with the same values of I_s, I_L and T. It can be seen that a shunt resistance as low as 100 ohms does not appreciably change the power output of a unit, whereas a series resistance of only 5 ohms reduces the available power to less than 30% of the maximum power with $R_s = 0\ \Omega$. Hence, the effect of R_{sh} can usually be neglected [20]. Under illumination, the output current is then described by:

$$I = I_o\left(\exp\left[\frac{q(V-IR_s)}{nkT}\right]-1\right)-I_L \qquad (8.4)$$

The series resistance of a cell is a combination of bulk semiconductor, metal contact and metal/semiconductor interface resistances. With our devices, any change in the illuminated I-V characteristic was, therefore, related to the back contact since this was the only difference between the cells.

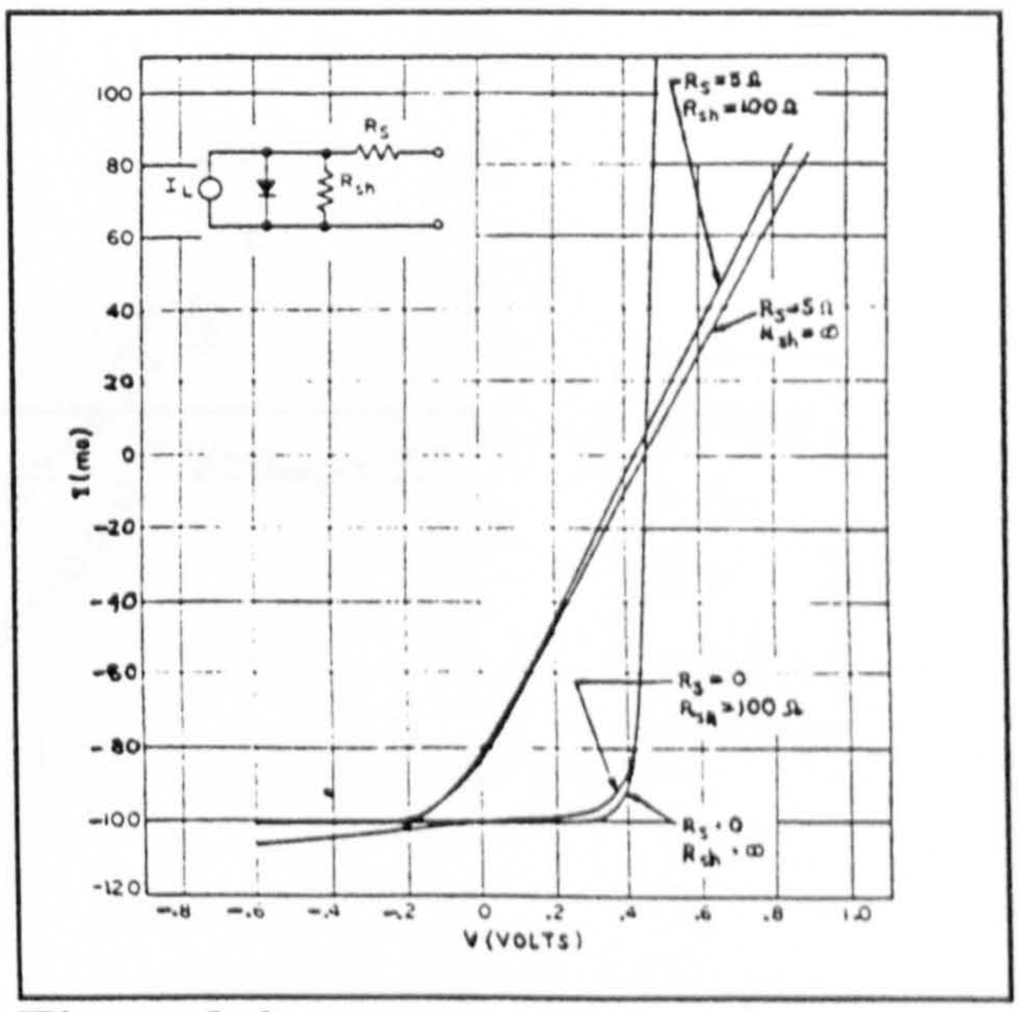

Figure 8.6 .. Theoretical I-V characteristics of various solar cells that include series and shunt resistances. The insert shows the equivalent circuit. (after Prince [22])

Table VIII.III lists the photovoltaic parameters of nominally identical CdS/CdTe cells equipped with different back contacts; Au, P, Sb, Cu and graphite. These results are for the same cells used to obtain the dark characteristics shown in figure 8.4. The quoted efficiencies need some qualification and should be viewed as relative values because the illuminated area was not well defined. It is quite clear that both Cu and P contacts to p-CdTe give much higher short circuit currents (I_{sc}), better open circuit voltage (V_{oc}) and

Table VIII.III .. Photovoltaic parameters of differently contacted CdS/CdTe:P solar cells.

Contact	V_{oc}	I_{sc}	FF	eff.
Au	0.316	$2.1e^{-5}$	0.31	1.37
P	0.469	$1.2e^{-4}$	0.34	12.9
Sb	0.413	$3.5e^{-5}$	0.31	3
Cu	0.457	$1.5e^{-4}$	0.31	14.1
Graphite	0.417	$3.7e^{-5}$	0.32	3.32

consequently conversion efficiencies (η), than the others. It was concluded, therefore, that work should be concentrated on these two elements for ohmic contact formation to CdTe:P.

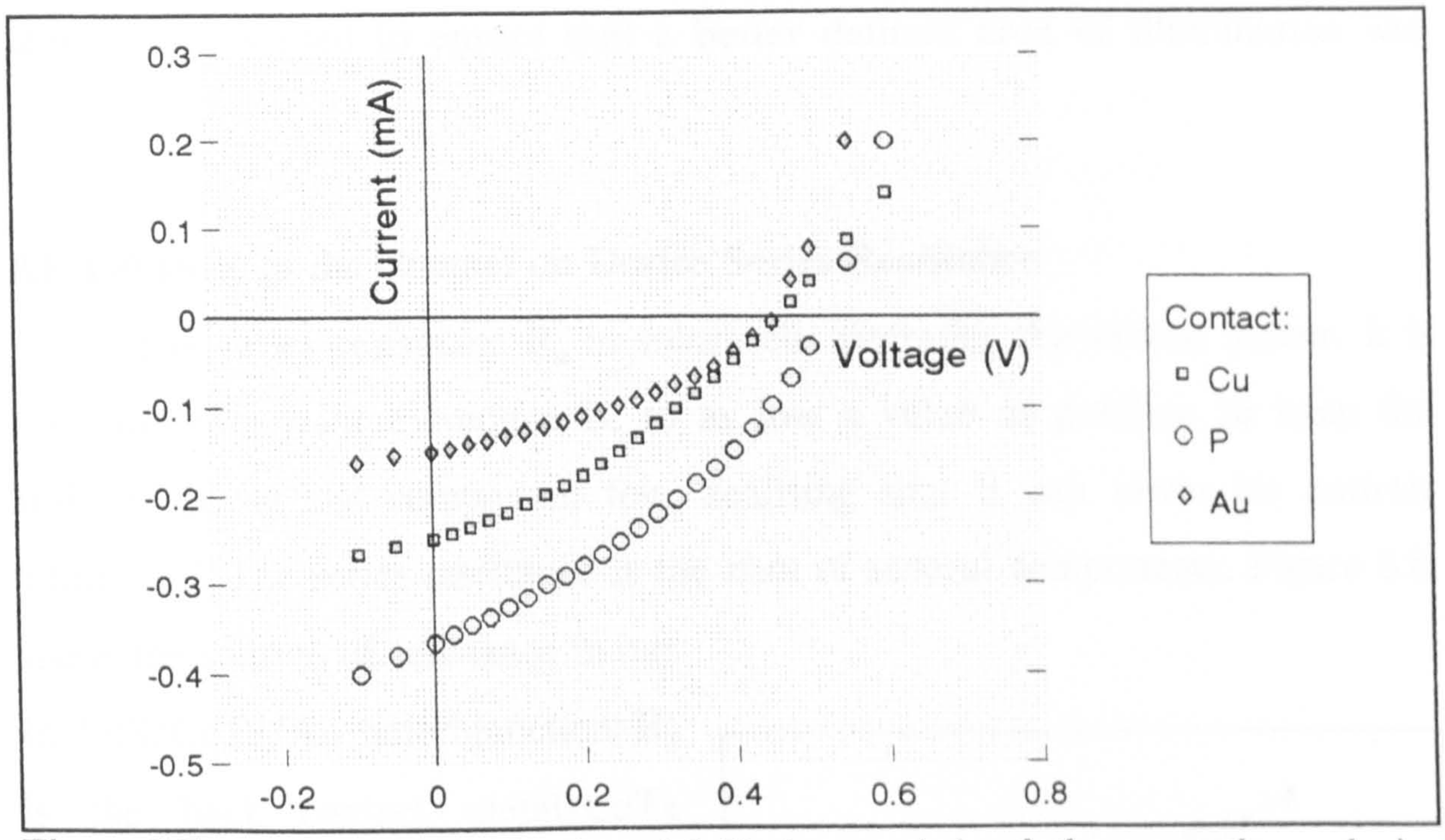

Figure 8.7 .. A plot of the illuminated I-V characteristic of the same three devices given in Figure 8.4.

The results from the second series of trials, using Au, Cu and P, with the same samples used to obtain figure 8.5, are given in table VIII.IV. A plot of the illuminated current-voltage characteristics of the three cells is shown in figure 8.7. Although gold gave a slightly higher fill factor, the output power suffered from the much lower short circuit current. Resistance effects were more pronounced with Cu than with P, giving a low fill factor and a low slope in the first quadrant of the I-

Table VIII.IV .. Photovoltaic parameters of three CdS/CdTe heterojunction using different back contacting materials.

Contact	I_{sc}	V_{oc}	FF	eff.
Au	$1.5e^{-4}$	0.46	0.37	2
Cu	$2.6e^{-4}$	0.46	0.31	2.9
P	$3.6e^{-4}$	0.51	0.36	5.1

V characteristics. The P contacted device gave the highest efficiency; with higher I_{sc} and V_{oc}, although the FF was still poor. The values of efficiency listed in table VIII.IV are more reliable than those in table VIII.III because a masking technique was used to ensure that a better defined area of illumination was obtained.

8.6. Influence of the Contact on Device Series Resistance

The series resistance R_s in solar cells degrades the output power. It is therefore important to reduce R_s to as low a value as possible to keep the resistive power-loss component low, realising that it can never be entirely eliminated. The series resistance is the sum of several components. Figure 8.8, shows the sources of resistance in our In/CdS/CdTe/Au heterojunction; R_1 is the back contact metal/CdTe resistance; R_2 is the CdTe:P substrate resistance; R_3 is the undoped CdS sheet resistance, and R_4 is the CdS/In top contact resistance.

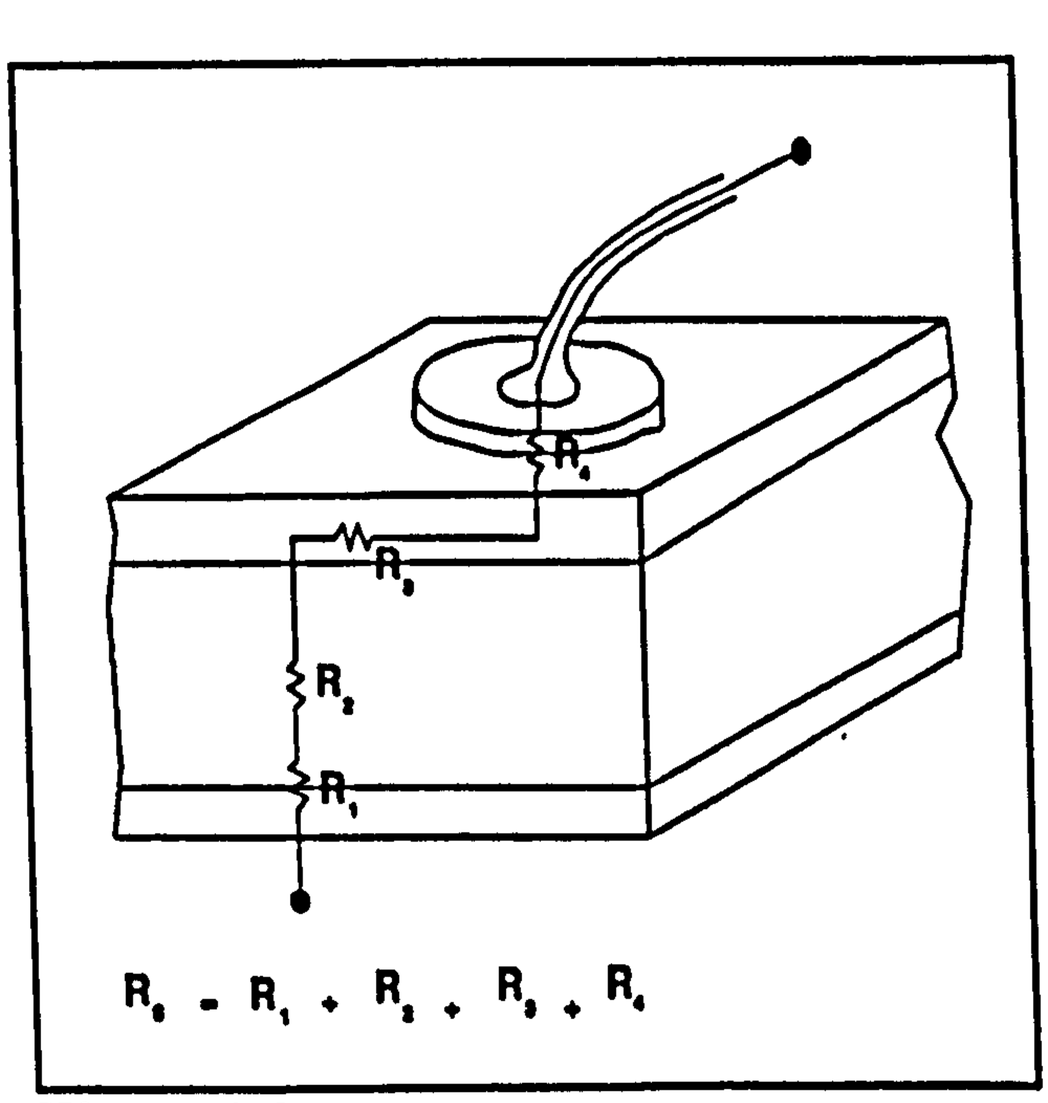

Figure 8.8 .. CdS/CdTe solar cell series resistance components.

The internal series resistance of a solar cell can be measured using the photovoltaic effect. Any change in the light intensity changes the photovoltaic relationship (equation 8.4) through the light generated current I_L. The internal series resistance is obtainable by measuring the photovoltaic output characteristics at two different light intensities, the magnitude of which do not have to be known. It can be proved, if shunt resistance losses are small (see chapter 5), that the two characteristics are translated relative to one

other by the amounts ΔI_L and $\Delta I_L x R_s$ in the y- and x-directions, respectively. The value of the internal resistance R_s is obtained from a displacement of two corresponding points on the two characteristics which give the values of ΔI_L and $\Delta I_L R_s$ parallel to the ordinate and parallel to the abscissa, respectively [21]. Using this approach, but noting that the contact resistance is a component of the internal series resistance of a cell, calculated resistances would give values that are in fact related to each other by the variations introduced by the different methods of forming the back contacts for otherwise identical cells.

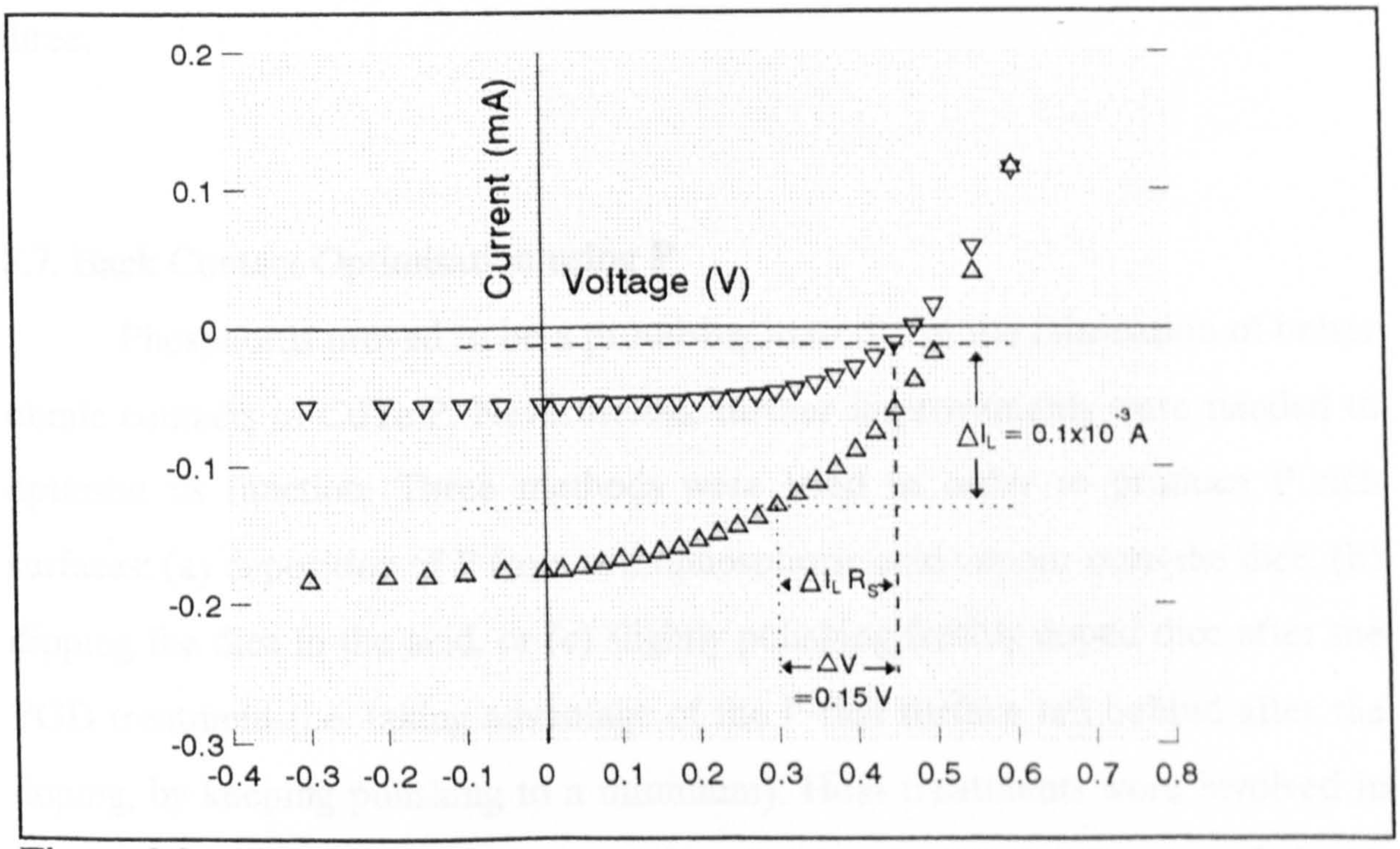

Figure 8.9 .. Illuminated I-V characteristics of the same CdS/CdTe solar cell at two different illumination levels. Such measurements are useful in determining device series resistance.

Figure 8.9 demonstrates the method for a CdS/CdTe solar cell with P as the contacting p^+ element. The calculated series resistance for the cell shown is ≈ 1250Ω. Such a high value would undoubtedly result

Table VIII.V .. Internal parameters of identical CdS/CdTe solar cells made with different back contacts.

Contact	R_s	FF	eff.
P	1250	0.42	4.5
Au	2071	0.45	1.8
Cu	2250	0.36	1.1

in a significant reduction in the fill factor (0.42 in this case) and would also limit the conversion efficiency (4.5%). Taking into account the use of highly resistive bulk CdTe and an undoped CdS thin film, to prepare the junctions, it is not surprising perhaps that this is so large. The corresponding calculated resistances for identically fabricated cells, which differ only in the methods of contacting with Au and Cu, were 2071 Ω and 2250 Ω, respectively. These three R_s values are in line with the calculated fill factors and conversion efficiencies of the same devices, see table VIII.V. Oddly, the FF with the Au gold contract was the largest of the three.

8.7. Back Contact Optimisation using P

Phosphorus proved to be a promising material in the fabrication of better ohmic contacts to CdTe:P. Nevertheless, further improvements were needed to optimise its function. Three methods were tried in order to produce P rich surfaces: (a) deposition of P from orthophosphoric acid vapour onto the dice, (b) dipping the dice in the acid, or (c) slightly polishing freshly doped dice after the PGD treatment (i.e. taking advantage of the P-rich surface left behind after the doping, by keeping polishing to a minimum). Heat treatments were involved in the first two methods only, where one, two, or four hour anneals were tried with (a) and a two hour anneal with (b). These heat treatments, if any, were carried out prior to the CdS deposition. Apart from those variations, cells were fabricated as described in section 8.3, without further heat treatment after junction formation. Photovoltaic output and diode characteristic (I-V analysis) were used to assess the results.

Dark and illuminated I-V characteristics of tested cases are shown in figure 8.10a and b, respectively. A summary of photovoltaic and diode parameters is also given in table VIII.VI. For the cell with P deposited (type a) onto CdTe:P, it is

obvious that the prolonged annealing time of evaporated P increases the short circuit current and hence conversion efficiency. In contrast, successive heat treatments tend to have unusual effects on the diode ideality factors. Dice dipped into the acid and then annealed for 2 hours tend to have effects similar to those with type (a) contacts annealed for the same time, though two interesting differences should not be overlooked; a higher open circuit voltage and lower reverse saturation current. These may be due to a highly doped interface with CdS; in the dipping process the acid attacks both surfaces of the CdTe dice. In the slightly polished device, benefit has been derived from the existence of high doping concentrations at both surfaces, where higher doping of the interface with CdS tends to lead to higher V_{oc} and higher doping at the back contact with Au

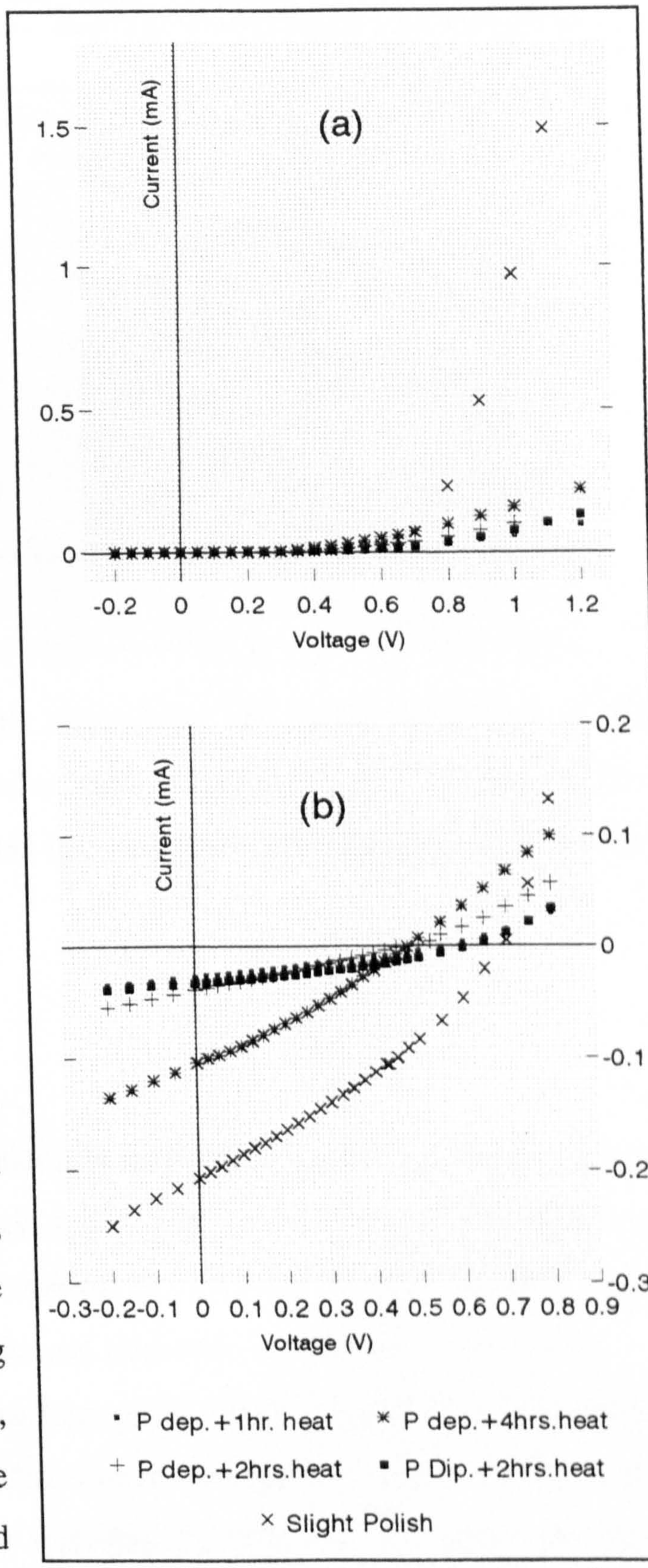

Figure 8.10 .. Dark; (a) and illuminated;(b) I-V characteristics of five different devices used in the optimisation of P contacts to p-CdTe.

Table VIII.VI .. Photovoltaic and diode parameters of five similar CdS/CdTe solar cells made with different P deposition and treatment method.

P deposition & treatment method	Photovoltaic				Diode	
	I_{sc}	V_{oc}	F.F.	eff.	n	I_o
Evap.& 1hr.Ann.	$2.7e^{-5}$	0.57	0.28	0.93	1.6	$5.1e^{-8}$
Evap.& 2hr.Ann.	$3.9e^{-5}$	0.48	0.26	1.02	1	$1.1e^{-9}$
Evap.& 4hr.Ann.	$1.0e^{-4}$	0.48	0.3	3.07	0.8	$6.8e^{-9}$
Dip.& 2hr.Ann.	$3.3e^{-5}$	0.62	0.33	1.42	1.3	$3.7e^{-7}$
Slightpolishafter PGD treatment.	$2.1e^{-4}$	0.7	0.32	9.43	1.1	$9.2e^{-9}$

results in a higher I_{sc}. It is worth highlighting the beneficial effects of this procedure on the diode parameters in spite of a rather low fill factor. Using a defined effective area for this last cell, a conversion efficiency of 9.4% was achieved.

8.8 Discussion and Conclusion

In most of our contact studies it is clear that a simple treatment of the p-type CdTe surface does introduce a p^+ layer at the contact-CdTe interface. Several contacting procedures involving Sb, Cu, Au, P, and Graphite, were applied to nominally identical cells and subjected to extensive investigation.

In this work P has given the best results relative to the other investigated materials. However, further investigations are needed to optimise the deposition and annealing conditions of these materials, for instance, to examine the effect of introducing Au before or after the junction formation. The introduction of gold before the CdS deposition, when it was annealed for around 4½ hours gave worse

results than when a 2 hour anneal was used. This could imply an excess of Au at the interface where it introduces interstitial donors in the matrix. Although graphite has proved to be useful for the formation of ohmic contacts to CdTe, its further investigation was suspended because of the desirability of eliminating unknown impurities from the complex. Measured series resistances gave further support to the superiority of P in the ohmic contact formation process.

Several applications and treatments with phosphorus were studied. These indicated further success is most likely to be obtained by using the (<1 mm) PGD process doped CdTe and removing the highly damaged part of the surface with a slight polish. We expect this method to provide competitive conversion efficiencies. Of course, the stability of these devices remains to be investigated. Further analysis of efficient CdS/CdTe solar cells is discussed in the next chapter.

8.9. References

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Chapter IX

CdS/CdTe:P Solar Cells

9.1. Preface

The CdS/CdTe heterojunction only holds promise as a low cost terrestrial solar cell in thin film form. Nevertheless, studies of bulk crystal cells are useful in obtaining a basic understanding of the junction properties, and of the effects of various material parameters without the added complication of grain boundaries, etc. Thus while not commercially viable devices, bulk crystal structures do serve as a guide to future thin film work.

The properties of optimised photovoltaic cells are described and investigated in this chapter. This investigation includes: dark and illuminated current-voltage (I-V), capacitance-voltage (C-V), photoresponse (PR), and electron beam induced current (EBIC) measurements. Moreover, as part of the internal parameters of the device, series (R_s) and shunt (R_{sh}) resistances were obtained from a detailed analysis of the open circuit voltage and a short circuit current relations. A comparative study of the effect of the bulk CdTe resistivity was carried out in terms of both illuminated and dark I-V characteristics. The results are compared with published data.

9.2. Fabrication Process

Post-growth doped (PGD) CdTe dice (see chapter 6) were used as the p-type substrates in the CdTe/CdS solar cells. Optimised back contacts to CdTe:P were used, which involved slightly polishing a freshly treated dice, such that phosphorus served as the dopant in both the CdTe bulk and in the p^+ layer formed at the back surface underneath the gold metallic contact (see chapter 8).

To create the heterojunction, a CdS layer, about 0.8 μm thick, was vacuum deposited onto the CdTe. Indium was used as the top contact to the CdS window layer and was deposited in two steps; firstly, a thin transparent layer of In was deposited onto the CdS to cover the whole device area, then secondly, a small thick spot was evaporated to the middle of the top surface, for use as a contact pad to which the leads were to be connected. The thin In layer provided a relatively large conduction area, and helped in offsetting the high sheet resistance of the undoped CdS. Excess CdS and/or In were removed from device edges by a concentrated HCl etch. Solar cell effective area was defined by a square opening in an opaque adhesive tape, and the effective area was calculated by subtracting the area of the thick In spot from the un-covered space of the device. In spite of the use of undoped CdS and the absence of any heat treatments for either the CdS junction, or the top contacts, a conversion efficiency of 9.5% was obtained with a high open circuit voltage.

9.3. Heterojunction behaviour of p-CdTe:P/n-CdS cells

9.3.1. Room Temperature I-V and C-V Characteristics

The diode characteristic of a solar cell fabricated on a slightly polished CdTe:P dice (after being treated in the PGD process) is shown in figure 9.1. The diode was clearly rectifying, with a rectification ratio of 4.9×10^3 at a bias of one volt. The ideality factor (n) was calculated to be 1.5, indicating that the heterojunction was well formed, in spite of the polycrystalline nature of the CdS layer. The value of the reverse saturation current I_o was 4.82×10^{-9} A; for such a low reverse saturation current, a high open circuit voltage would be expected.

The capacitance as a function of voltage for the heterojunction is given in figure 9.2. A value of 0.61 eV was found for the diffusion voltage V_D while from

the slope, the free carrier concentration in the CdTe was estimated to be in the range of 10^{16} cm^{-3}. The intercept on the C^{-2}-axis, gave a value of 0.22μm for the depletion region width. This assumes a one-sided junction in which all the depletion region was located in the CdTe:P. The validity of this assumption is open to question, since the resistivity of the CdS was unknown, but thought to be high as it was undoped. Test layers of CdS deposited on glass were found to be resistive and resulted in values of the Hall coefficient that were not meaningful. Similarly the use of freshly doped CdTe in the cell fabrication prohibited any prior analysis of the CdTe substrate. Consequently, using the C-V characteristics to estimate the carrier concentration in the CdTe:P (besides the effect of interface states on the capacitance of the p-n heterojunction which have been neglected) could lead to substantial error. The EBIC measurements discussed below (section 9.3.2) suggest that a significant fraction of the junction space charge region may have been supported in the CdS. However, this appears to be in conflict with the photoresponse measurements (section 9.4.2), these show a conventional window response with no appreciable enhancement at the CdS band edge,

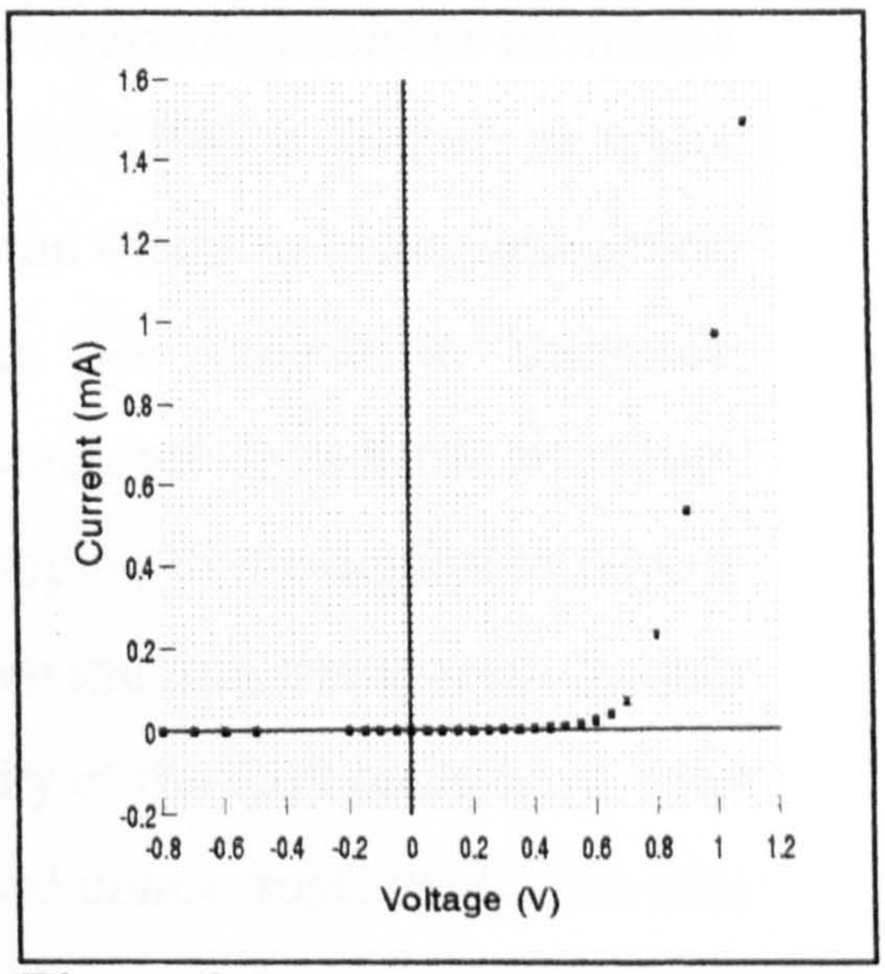

Figure 9.1 .. Dark I-V characteristic of a CdTe:P/CdS heterojunction. The device was fabricated on PGD treated CdTe with a p^+ layer at the back contact.

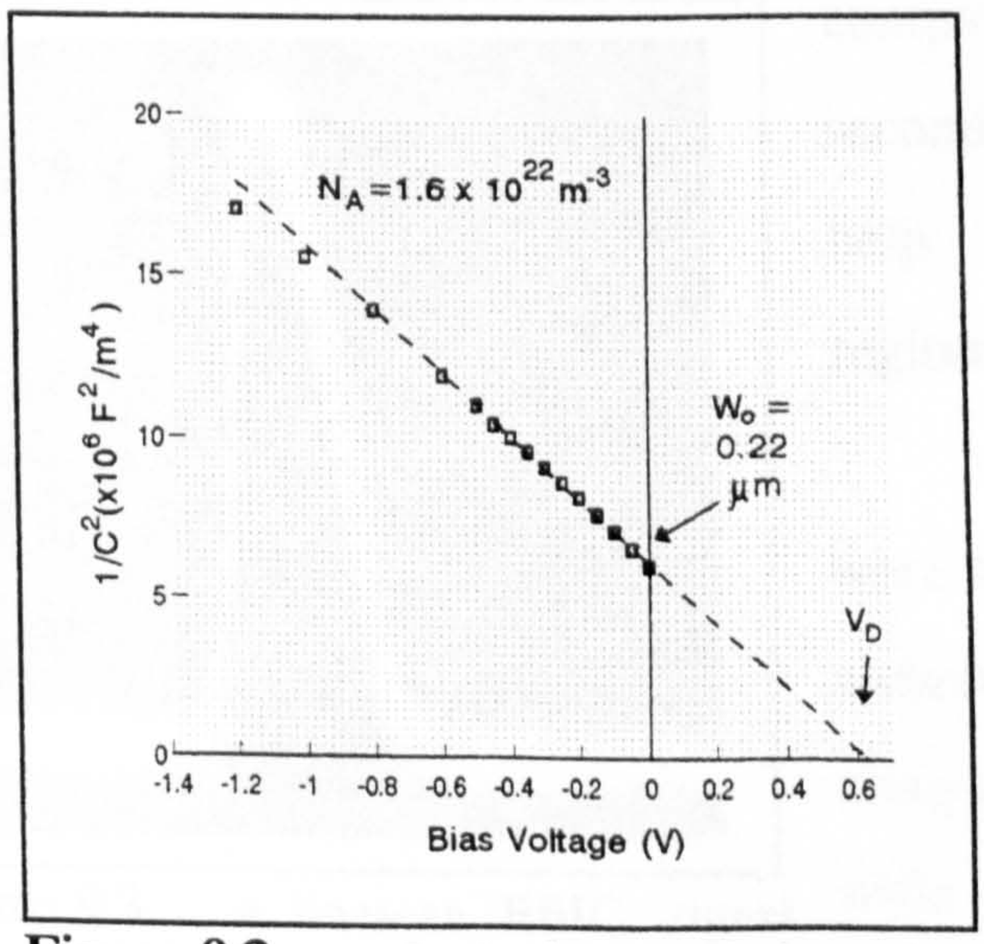

Figure 9.2 .. C-V characteristic of a CdTe:P/CdS heterojunction. The linear relationship, indicates an abrupt interface between the two semiconductors.

implying little or no depletion in the CdS layer. Unfortunately, neither technique is definitive in this respect. The spatial resolution of EBIC is limited to scales comparable with the expected depletion width by the electron-beam interaction volume, while the photoresponse characteristics are subject to uncertain recombination losses. Nevertheless, the C-V measurements do indicate an abrupt junction at the interface with apparently uniform doping in the depletion region. It is possible that there was some diffusion of In from the thin transparent contact into the CdS. If this had occurred, then the resistivity of the CdS could have been greatly reduced as In (i.e. group III dopant) is a good donor impurity. In this case the depletion region would be fully in the CdTe side.

9.3.2. Depletion Width and Minority Carrier Diffusion Length

Measurement of the minority carrier diffusion length is important in order to determine the volume of the semiconductor near the junction, from which light generated carriers may be collected. Diffusion length is readily measured using the EBIC technique in the SEM [1,2,3] as described in chapter 5. EBIC may also used to image potential barriers, and comparison with the corresponding secondary electron (SE) image can often help in identifying electrically active regions.

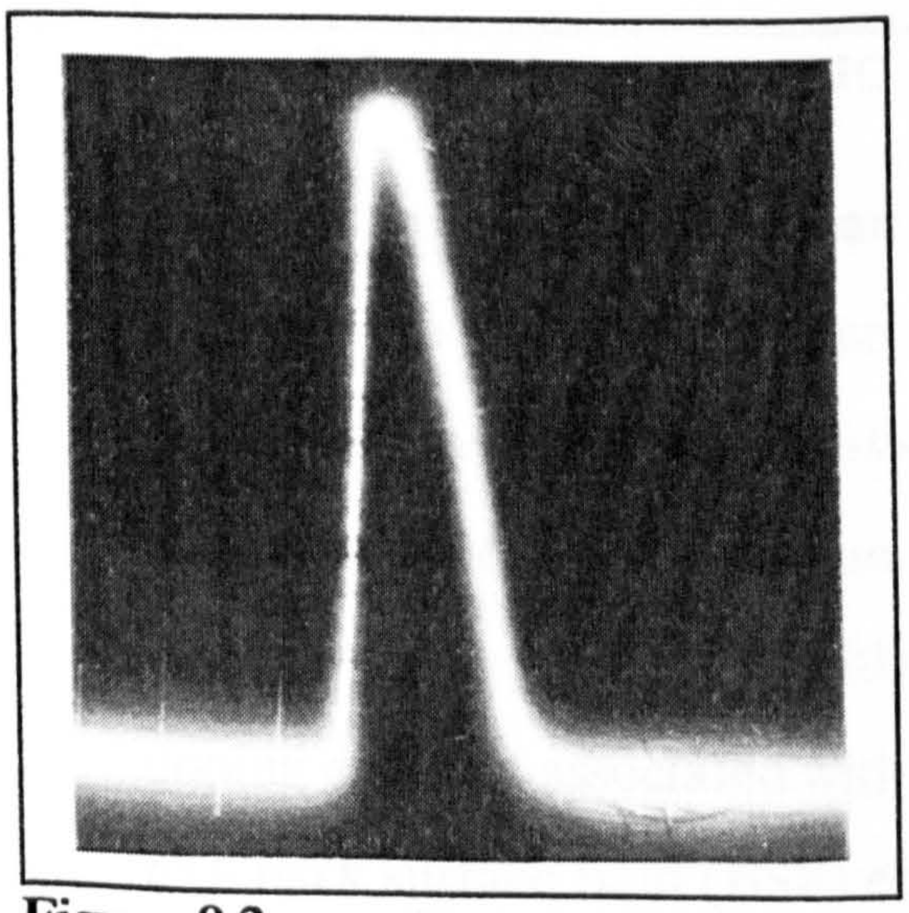

Figure 9.3 .. A linescan EBIC signal across a cleaved CdTe:P/CdS junction. Where the CdTe is to the right of the peak.

The diffusion length measurements were made using a single line scan across a cleaved section through the junction and analysed (see chapter 5) in accordance with;

$$J_n(x) = J_o \exp\left(\frac{-x}{L_n}\right) \qquad (9.1)$$

All the measurements were made with a beam energy of 25 KeV, to ensure that surface recombination effects could be neglected. However, the generation volume will be correspondingly larger , resulting in a loss of spatial resolution.

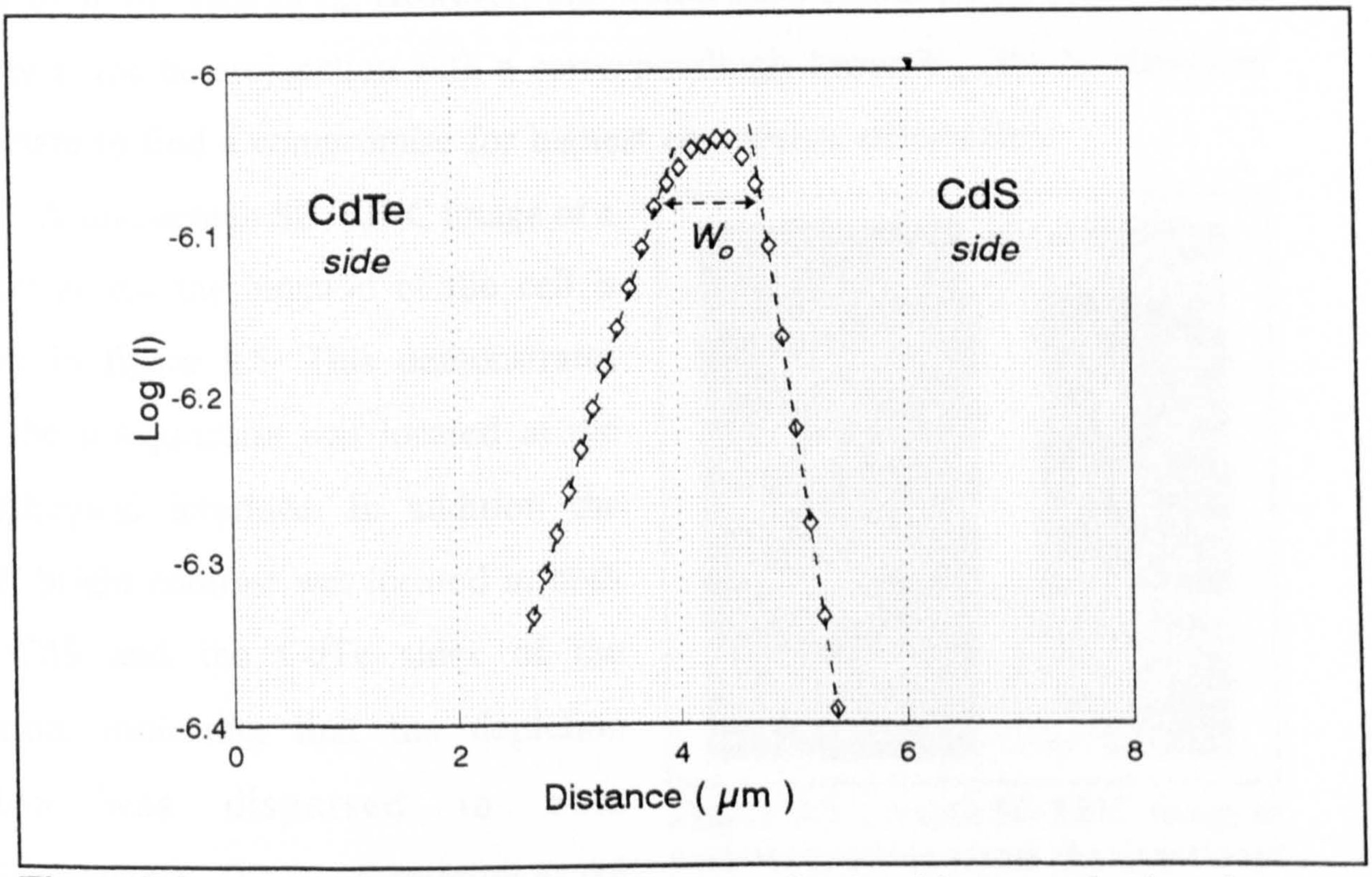

Figure 9.4 .. A plot of log EBIC current versus distance (x) across the junction.

A typical EBIC linescan of the solar cell is shown in figure 9.3. A plot of log response vs x the distance across the junction for the linescan is shown in figure 9.4. The values of diffusion length L_n (in CdTe) and L_p (in CdS) obtained from the slopes were 1.95 μm and .86 μm respectively. Interestingly, a similar device without p^+ layers at either side gave a larger value of 2.25 μm for L_n. The doping gradient associated with the creation of a p^+ surface layer should give rise to a back surface field (BSF) effect leading to an increase in the measured value of L_n. In the present case, where the post-doping polishing was kept to the minimum (section 8.7), there may well have been a relatively high density of

surface and near-surface crystallographic defects remaining after the PGD treatment (section 6.5). The increased rate of recombination would offset (and seemingly did so) any increase in measured L_n due to the effects of BSF. Further polishing might have reduced the number of recombination centres near the heterojunction leading to an increase in minority carrier diffusion length and hence to an increase in I_{sc}, However, this would have resulted in a lower doping density at the heterojunction with a correspondingly lower V_{oc}. It was therefore important to find a compromise for highest conversion efficiencies.

A split-screen SE/EBIC image of a section across the junction of the cell is shown in figure 9.5. This demonstrates that the p-n junction was located at the metallurgical interface. In addition the EBIC bright contrast was located in both the CdS and the CdTe sides of the junction, indicating that the depletion region was dispersed in both semiconductors. The p-n formation at the metallurgical interface confirms a true heterojunction rather than a buried homojunction, this observation agrees with previous reports [4,5].

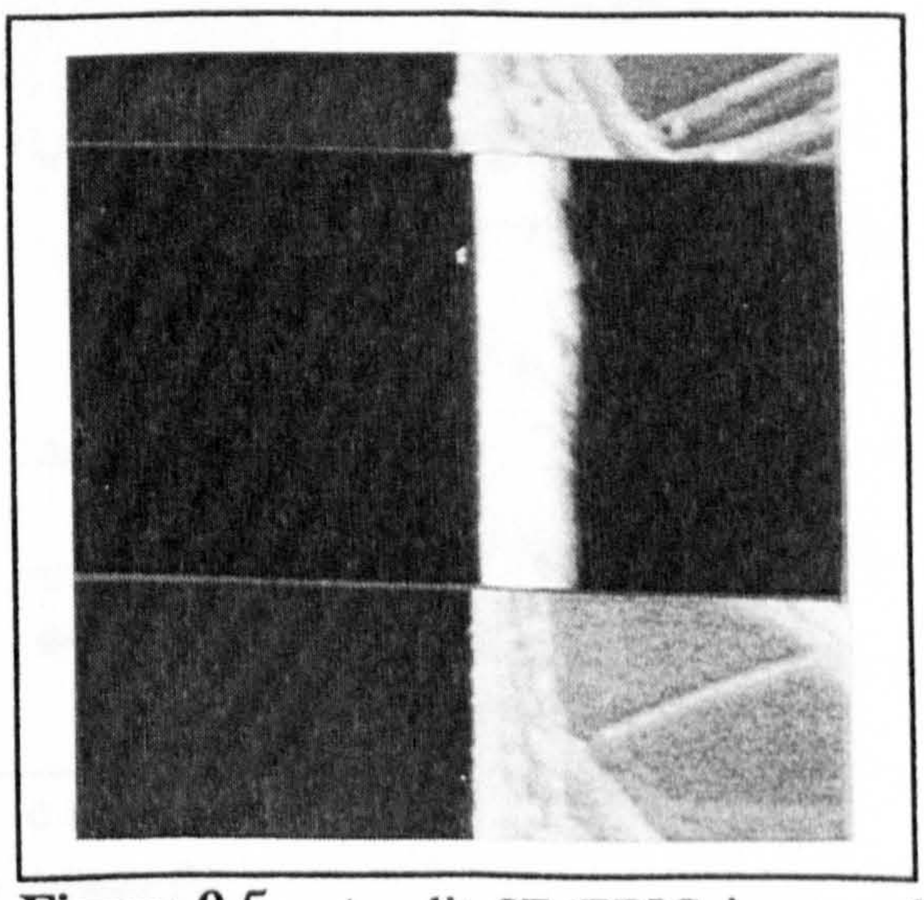

Figure 9.5 .. A split SE/EBIC image of a cleaved section across the junction of the same device (Figure 4 & 5). Where CdTe is at the right hand side

The depletion region width (W_o) can also be obtained from the EBIC measurements. The characteristics of figure 9.4 give a value of 0.9 μm for W_o, four times that (0.22 μm) obtained from the C-V characteristics. As indicated previously the spatial resolution of EBIC is limited, and the estimate of 0.9 μm for W_o is probably subjected to smearing (due to the comparable electron-beam interaction volume) and will therefore be an over estimate. On the other hand the small depletion width of 0.22 μm derived from the C-V results is related to the

large capacitance intercept value, suggesting that there was a significant amount of charge being trapped in interface states. It is, therefore, probably an underestimate. A high density of interface states is expected in the CdS/CdTe heterojunction, as a result of the large difference in lattice constant (~9.7%) which gives rise to unpaired valence band electrons or dangling bonds at the interface. Such states have a dramatic influence on capacitance measurements.

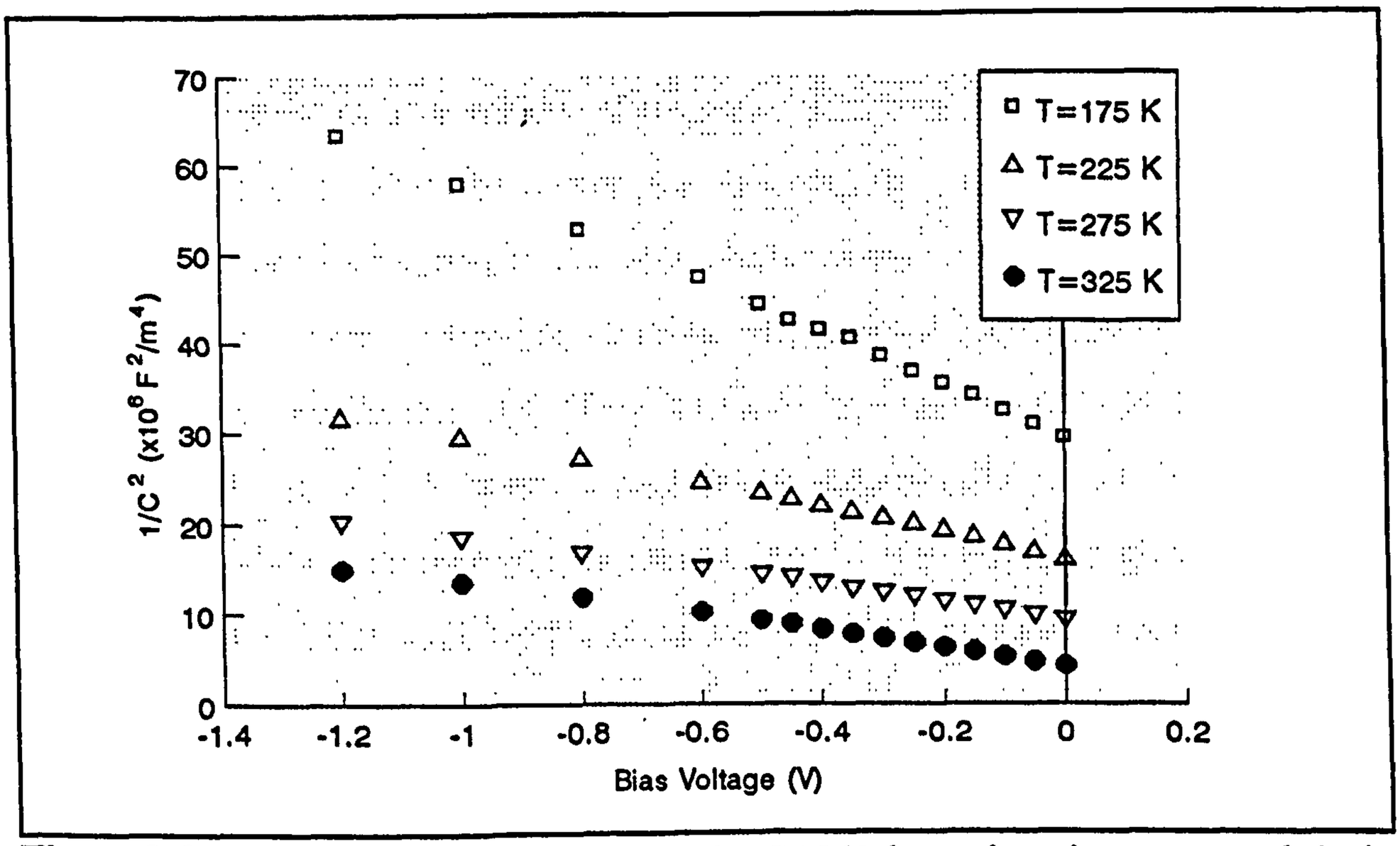

Figure 9.6 .. C-Vcharacteristics of the CdTe:P/CdS heterojunction at several device temperatures.

In order to investigate the variation of depletion width with temperature, capacitance-voltage characteristics were measured at several temperatures. Below a temperature of ~125K, it was found that the capacitance was essentially independent of the voltage. Above this temperature the C^{-2}-V plots were linear, (see figure 9.6), indicating that the junction was abrupt. Assuming a one sided junction the free carrier concentration in the CdTe would appear to have increased slightly with temperature (5.3×10^{15} cm^{-3} at 175 K to just over 1.6×10^{16} cm^{-3} at 325 K). Similarly, the depletion width decreased with increasing temperature (0.49 μm at 175 K to about .2 μm at 325 K) in a consistent manner.

This decrease was expected because of the increase in material conductivity as more carriers were released as the temperature was raised.

9.3.3. Current Transport Mechanisms in CdS/CdTe:P heterojunctions

9.3.3.1. Current Transport Mechanisms

In order to understand the behaviour of a diode, it is important to study its I-V characteristics at a variety of temperatures, from which a model for the current transport mechanism across the junction may be deduced. Many such models have been developed to describe charge transport mechanisms and more details may be obtained from [13]. Taking into account the existence of interface states and the heavily doped CdTe:P surfaces, the mechanisms relevant in the CdTe/CdS device include space charge recombination and tunneling processes. In the space charge recombination mechanism, it is assumed that the electrons and holes reach a defected interface via thermal processes and recombine there. This model may be described by

$$I = I_o \left[\exp\left(\frac{qV'}{nkT} \right) - 1 \right] \tag{9.2}$$

where V' the applied voltage and I_o, the reverse saturation current, is thermally activated and is given by the following relation;

$$I_o = I_{oo} \exp\left(\frac{-\Delta E}{kT} \right) \tag{9.3}$$

where I_{oo} is only weakly temperature-dependent. The value of n, the ideality factor in equation (9.2) is an indication of material and junction imperfection, and usually lies between 1 and 2. ΔE is a thermal activation energy.

On the other hand, tunneling mechanisms involve electrons tunneling

through the potential barrier between the two different materials in order to flow across the junction. This mechanism is represented by;

$$I = I_o \exp(A V^f) \tag{9.4}$$

where I_o, is an increasing function of temperature according to the relation;

$$I_o = I_{oo} \exp(BT) \tag{9.5}$$

where B is a proportionality constant. The above two expressions indicate that voltage and temperature appear as separate variables, where I_o is related exponentially to T (rather than 1/T).

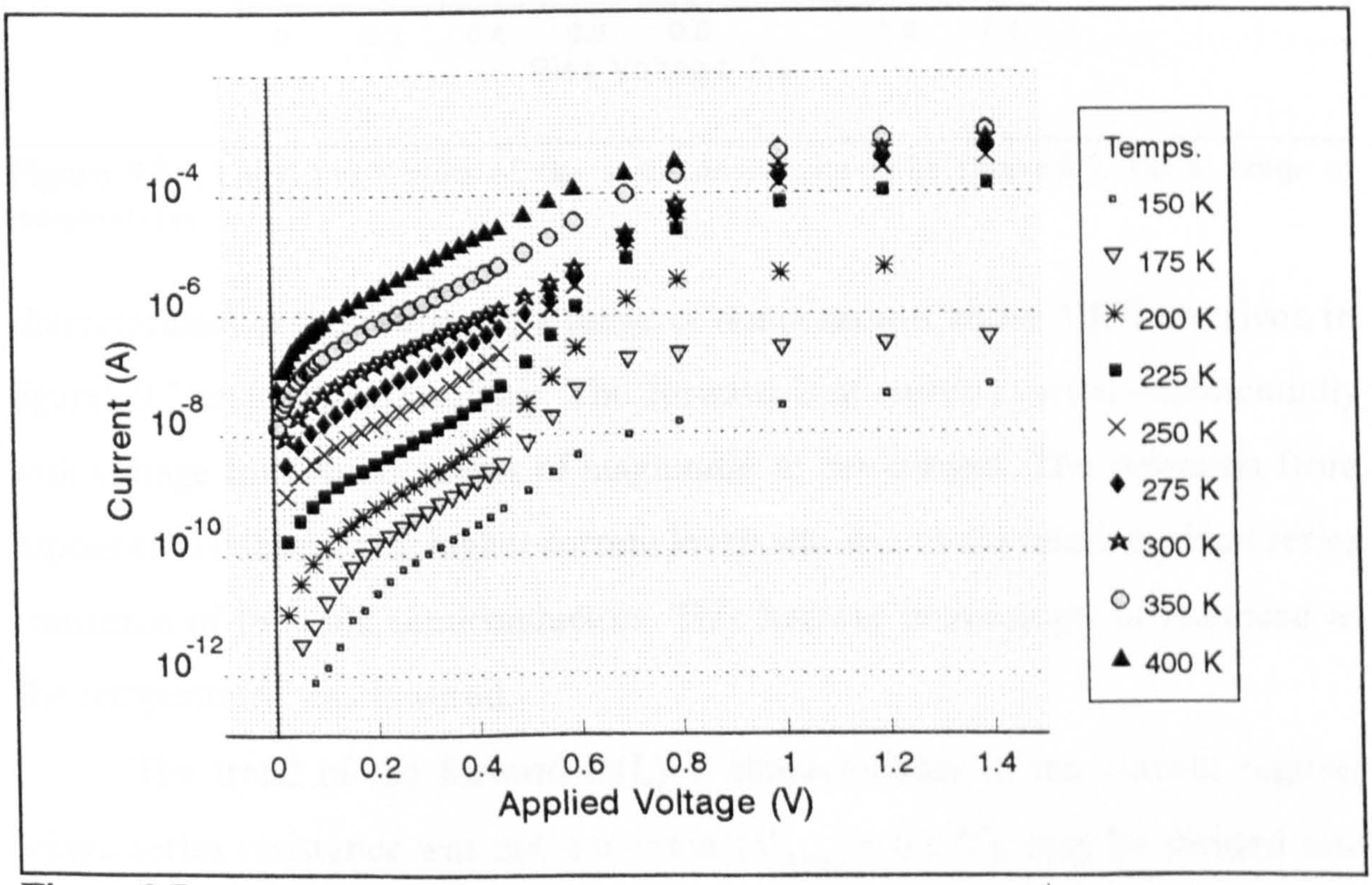

Figure 9.7 .. Log (I_f) vs V plots of a typical In-CdS/CdTe:P-P^+-Au solar cell for a range of temperatures.

In an attempt to investigate current carrying mechanisms in the CdS/CdTe solar cell, the I-V characteristics were taken for a range of temperatures from 77K to 400K. Below 100K there was no observable current above noise levels as the applied voltage was varied. The forward (I_f) and reverse (I_r) current-voltage

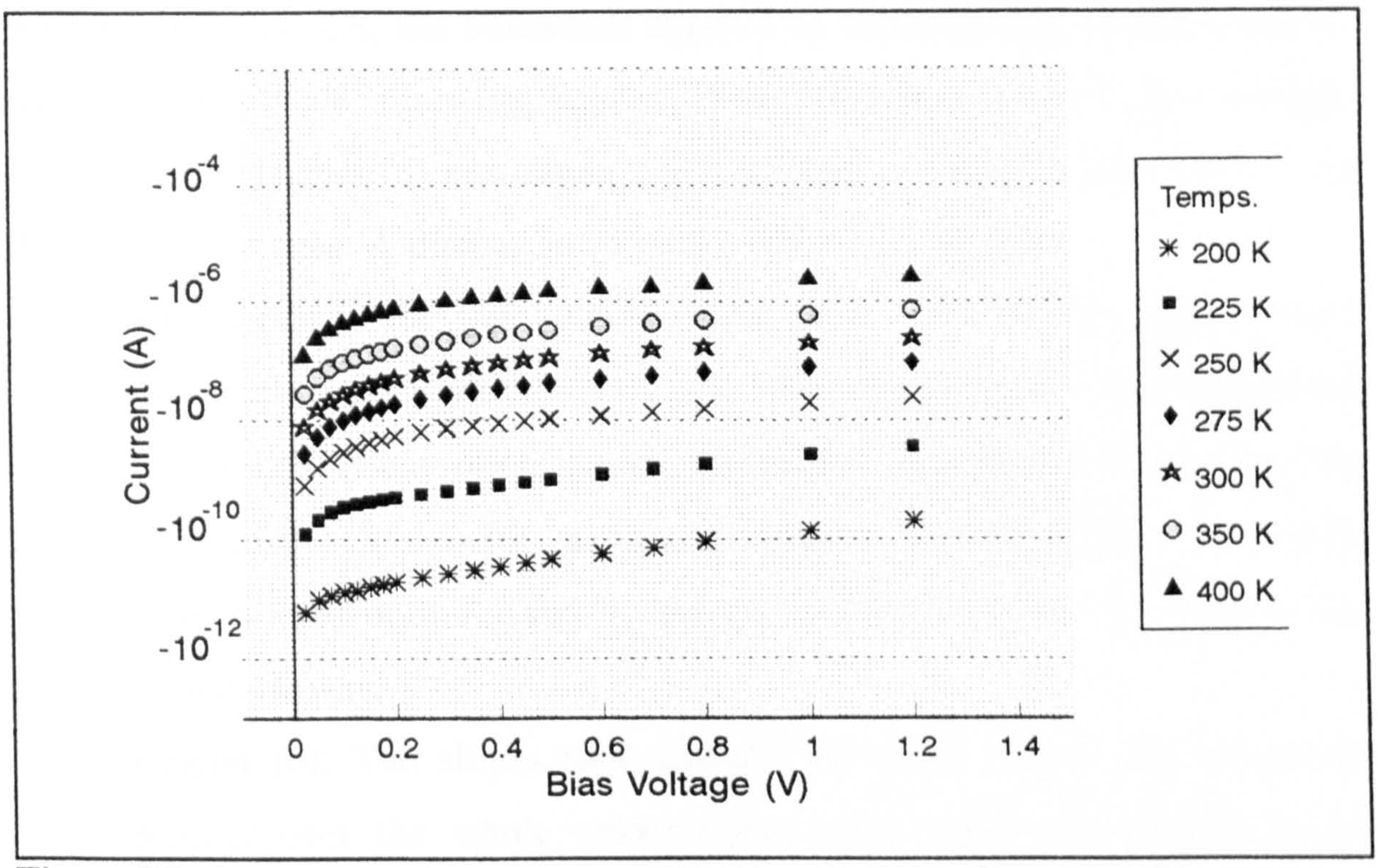

Figure 9.8 .. Log (I_r) vs V plots of the same device shown in figure 9.7, for a range of temperatures.

characteristics of the device for a range of temperatures above 100K are given in figures 9.7 and 9.8, respectively. The forward bias current varied exponentially with voltage for several orders of magnitude of the current. The deviation from exponential behaviour at higher current levels was due to the relatively high series resistance of the bulk semiconductors. This became increasingly pronounced as the temperature was lowered.

The trend of the forward $\ln(I_f)$-V characteristics in the current regime, where series resistance was not dominant ($V_{Appl} < 0.7$ V), may be divided into three regions. These three regions may be categorised in respect of the applied voltage as; (a) low voltage ($0.05 \leq V \leq 0.1$), (b) intermediate voltage ($0.125 < V < 0.425$), and (c) high voltage ($0.5 \leq V \leq 0.6$) ranges. Detailed diode parameters for all three voltage regions are shown in table IX.I. This has led to the assumption of a multi-diode model that could be used as an equivalent circuit for the heterojunction. At higher voltages before device series resistance takes over

the I-V characteristics, the behaviour appears to be controlled by space charge recombination, while tunneling appears to be important at lower bias voltages.

Ideality factors (n) and slopes (A) are listed in table IX.I for each of the three voltage ranges. A discussion of each region is as follows;

Region (a); In the low voltage range over ~250K the A_1 value (slope) varies only slightly with temperature, while the value of n decreased from 1.7 to 1.1. These observations are more consistent with a tunneling mechanism than with a space charge recombination. At lower temperatures both A_1 and n_1 are not constant but do not vary in any systematic way.

Region (b); The slopes vary slightly, but again not in any consistent manner over the whole temperature range, while the ideality factor

Table IX.I .. Analysis of the I-V vs. temperature characteristcs. where;a, b, and c correspond to applied voltage regions, (see text).

T (K)	region(a)			region(b)			region(c)		
	I_{o1}(A)	n_1	A_1	I_{o2}(A)	n_2	A_2	I_{o3}(A)	n_3	A_3
150	$4.6e^{-14}$	2.6	29.7	$2.6e^{-12}$	6.3	12.2	$1.7e^{-12}$	5.8	13.2
175	$6.3e^{-13}$	2.0	32.4	$1.4e^{-11}$	5.5	11.9	$3.1e^{-13}$	3.3	20
200	$4.6e^{-12}$	2.2	26.4	$6.5e^{-11}$	5.1	11.4	$6.2e^{-13}$	2.6	21.7
225	$1.0e^{-10}$	1.9	26.5	$4.0e^{-10}$	4.8	10.7	$3.8e^{-12}$	2.4	21.3
250	$4.6e^{-10}$	1.9	24.7	$2.0e^{-9}$	4.6	10	$7.2e^{-11}$	2.6	17.7
275	$1.5e^{-9}$	1.7	25	$6.9e^{-9}$	4.3	9.9	$1.6e^{-9}$	3.2	13
300	$4.8e^{-9}$	1.5	25.4	$2.7e^{-8}$	4.5	8.5	$8.2e^{-9}$	3.5	11
325	$7.6e^{-8}$	1.3	26.5	$5.3e^{-8}$	4.1	8.7	$1.7e^{-8}$	3.2	11
350	$1.9e^{-8}$	1.3	26.2	$1.0e^{-7}$	3.4	9	$3.4e^{-8}$	2.9	11.5
375	$5.1e^{-8}$	1.2	25.7	$1.8e^{-7}$	3.1	10	$1.3e^{-7}$	2.8	10.8
400	$8.3e^{-8}$	1.1	25.5	$3.0e^{-7}$	2.7	10.5	$3.8e^{-7}$	3	9.7

decreases with increasing temperature. These results suggest that there may be some tunneling mechanism associated with current transport in this voltage range.

Region (c); Apart from the value at 150K, the slopes are approximately constant up to 250K and decrease with increasing temperature above that. Values of n, fluctuate from 2.6 to 3.5 with an average value of about 3. This would imply that tunneling is more dominant at lower temperatures (T<250K), but at higher temperatures transport would appear to be more typical of space charge recombination.

However, the above results are not fully clear and it is necessary to study the temperature behaviour of the intercept values (I_o) which give a much better indication than the n and A approach. Figure 9.9 illustrates six plots of Log I_o versus T and 1/T for all three regions. The shapes of these curves indicate clearly that a transition in the behaviour is taking place at a temperature of ~ 250 K. Tables in figure 9.10 summarize the outcome of these observations. Proportionalities were easier to observe in the (a) and (b) voltage regions. For the region (c), where the device was operating near the series resistance dominated part of the I-V characteristics, it was more ambiguous. Plots 9(1,3) show that in regions (a) and (b) at low temperatures I_o varies exponentially with T, but that above this temperature it deviates from this behaviour. In region (c) there is no dependence at low temperatures (plot 9(5)). This implies that a tunneling transport mechanism was dominant in the low temperature range, and that the current followed a relation of the form shown in (9.4). On the other hand, plots 9(2,4, & 6) show that at high temperatures (T>250 °C) I_o varied exponentially (although this is less certain for region (c)) with 1/T, suggesting that a space charge recombination transport mechanism was more likely to be dominant, and the proposed I-V relation in this range was of the form given in equation (9.2). This would appear to be in conflict with the results of table IX.I. The discrepancy

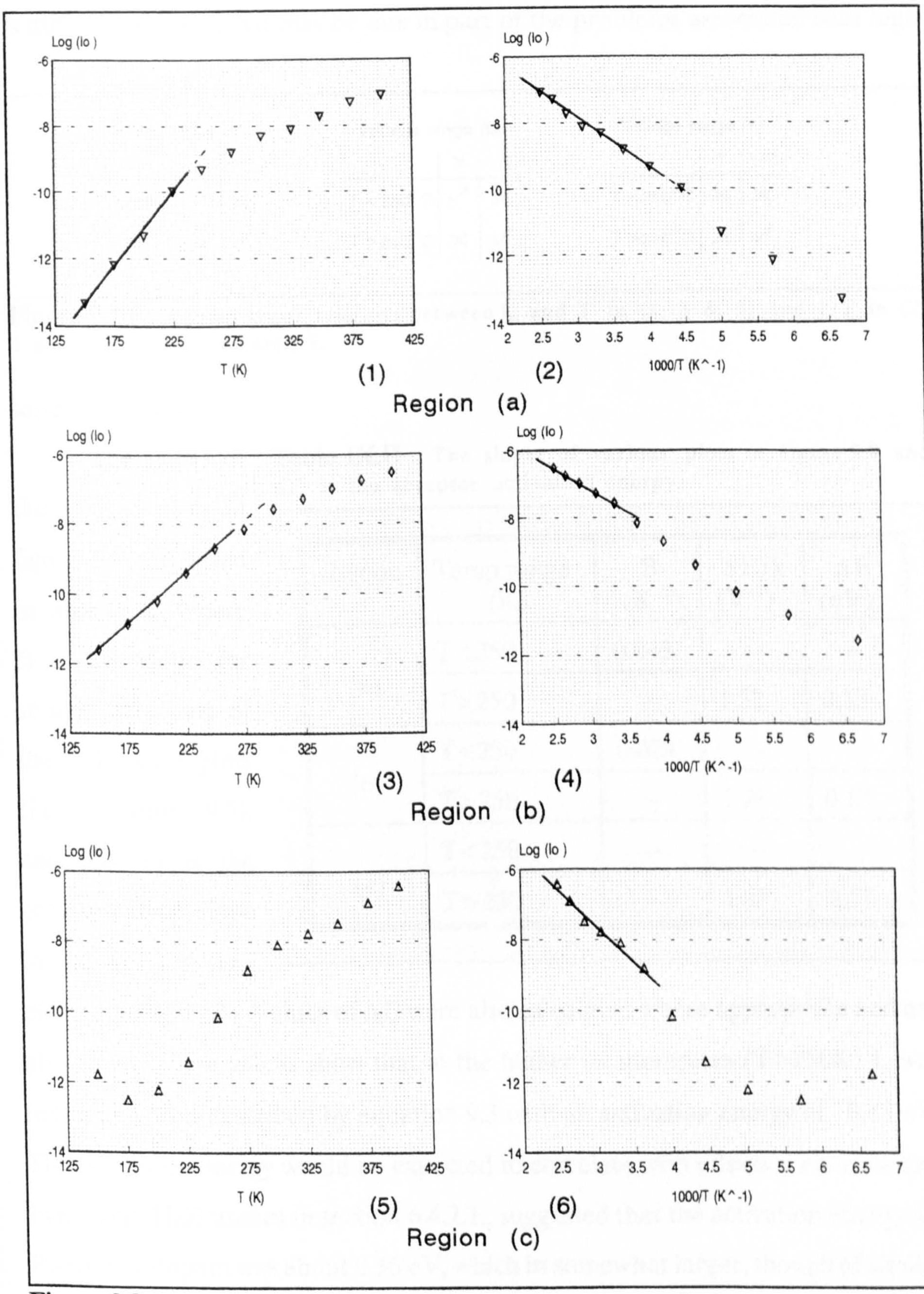

Figure 9.9 .. Plots of Log(I_o) versus T and 1000/T in three applied voltage regions of the CdS/CdTe:P I-V characteristics; where (1&2) for region (a), (3&4) for region(b), and (5&6) for region (c).

is difficult to explain but may be due in part of the problems associated with high

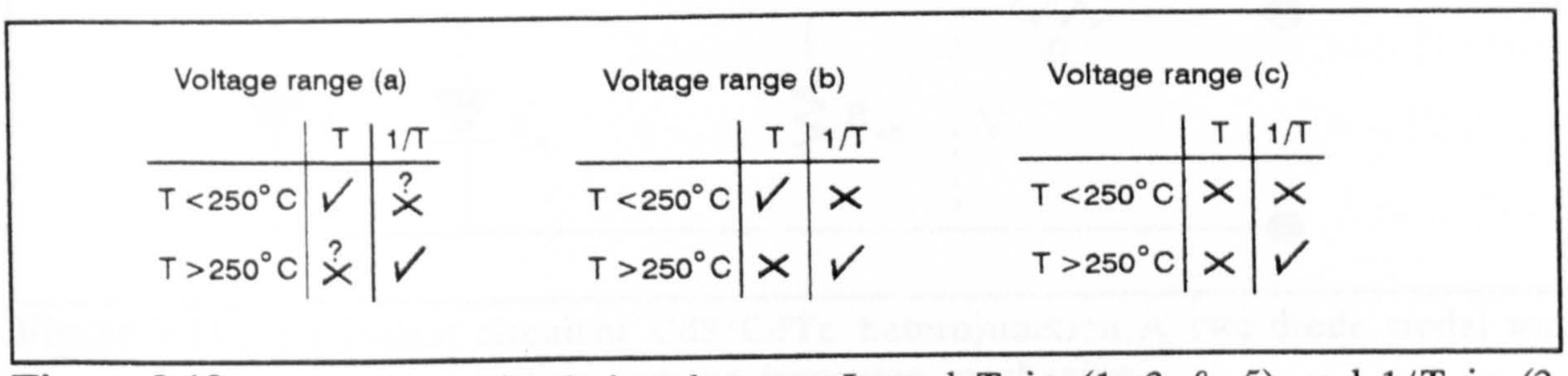

Figure 9.10 .. A summary of relations between I_o and T in (1, 3 & 5) and 1/T in (2, 4 & 6) of plots in figure 9.9.

series resistance.

The slopes of the various plots in figure 9.9 are listed in table IX.II. Where B is the slope for straight line part of the $\ln(I_o)$ vs T plots (i.e. equation 9.5), and ($\Delta E/k$) is the corresponding slope in the $\ln(I_o)$ vs 1/T plots (equation 9.3). Values of ΔE were also calculated where appropriate and are also listed. These values show that at the higher temperatures (T>250K) I_o was reasonably well described by equation 9.3 with an activation energy of ~0.13 eV. This activation energy would be expected to correlate with effects such as carrier freeze out. Hall studies in section 6.4.2.1., suggested that the activation energy for P acceptor dopant was about 0.36 eV, which in somewhat larger, though of similar magnitude. It should be noted that ΔE would also include other effects such as the temperature dependance of the mobility, etc. Interestingly, values of B are

Table IX.II .. The slopes of various plots in figure 9.9 and ΔE is the acceptor activation energy.

Region	Temp.range (K)	B (K^{-1})	$\Delta E/k$ (V^{-1})	ΔE (eV)
(a)	T<250	0.043	--	--
	T>250	--	1.52	0.13
(b)	T<250	0.029	--	--
	T>250	--	1.39	0.12
(c)	T<250	--	--	--
	T>250	--	1.97	0.17

comparable with published values [19].

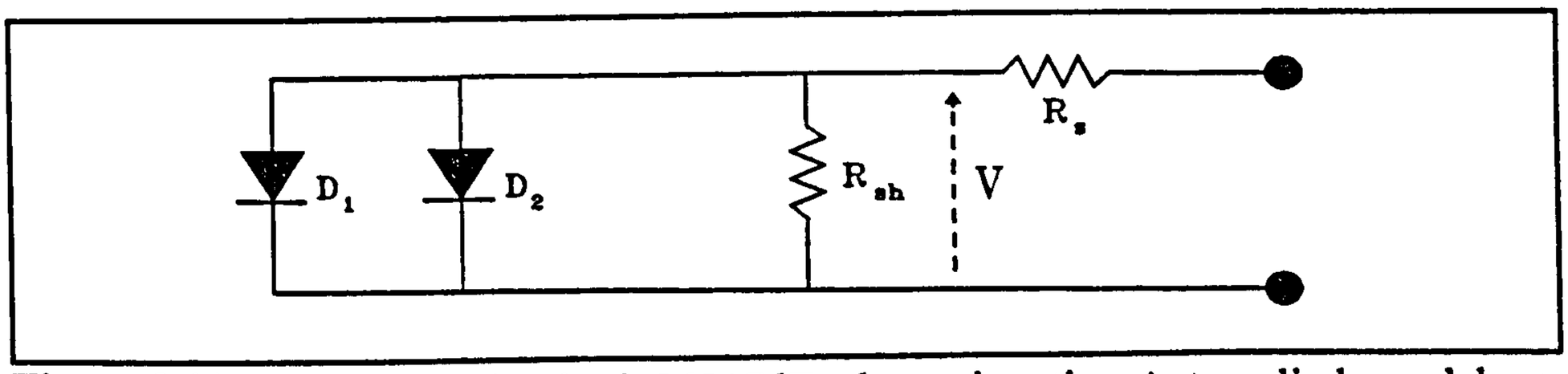

Figure 9.11 .. Equivalent circuit of CdS/CdTe heterojunction. A two diode model was proposed to investigate junction current transport mechanisms.

A proposed heterojunction equivalent circuit is portrayed in figure 9.11, incorporating two diodes in parallel, one dominant at low temperature is a tunnel diode the other represents the space charge recombination mechanism operative at higher temperatures. A general equation representing the current flow across the junction is of the form;

$$I = \sum_i I_i (V,T) \qquad (9.6)$$

where the Σ_i allows for the number of different mechanisms which add together to make the diode current, and I_i (V,T) corresponds to the current equations. Charge transport mechanisms for the diode, in summary, tend to change according to the temperature; where tunneling dominated at lower temperatures and space charge recombination controlled the current flow at high temperatures. Series resistance effects limited current flow at voltages over 0.7 volts.

9.3.3.2. Multi-step tunneling diode

Having found that in CdS/CdTe:P diodes a tunneling transport mechanism was dominating charge transport across the junction, it is of interest to further investigate such phenomena. Bringing equations (9.4) and (9.5) together, the tunneling expression [17] would be of the form;

$$I_f = I_{oo} \exp(BT) \exp(AV) \ldots (V>0) \quad (9.7)$$

where A is the tunneling constant and B gives the temperature dependence of the saturation current I_o. The net ionised acceptor density (N_A) in the CdTe was too low for direct band-to-band tunneling (this would require $N_A > 10^{17}$ cm^{-3}), but it is possible [18] for electrons to tunnel from the CdS into interband states at the interface, from where they may recombine with holes from the CdTe via a ladder of closely spaced states in the depletion region. A schematic diagram of such charge transport mechanism is shown in figure 9.12. The forward current in a multi-step tunneling/recombination model of this sort is given by [15,18]:

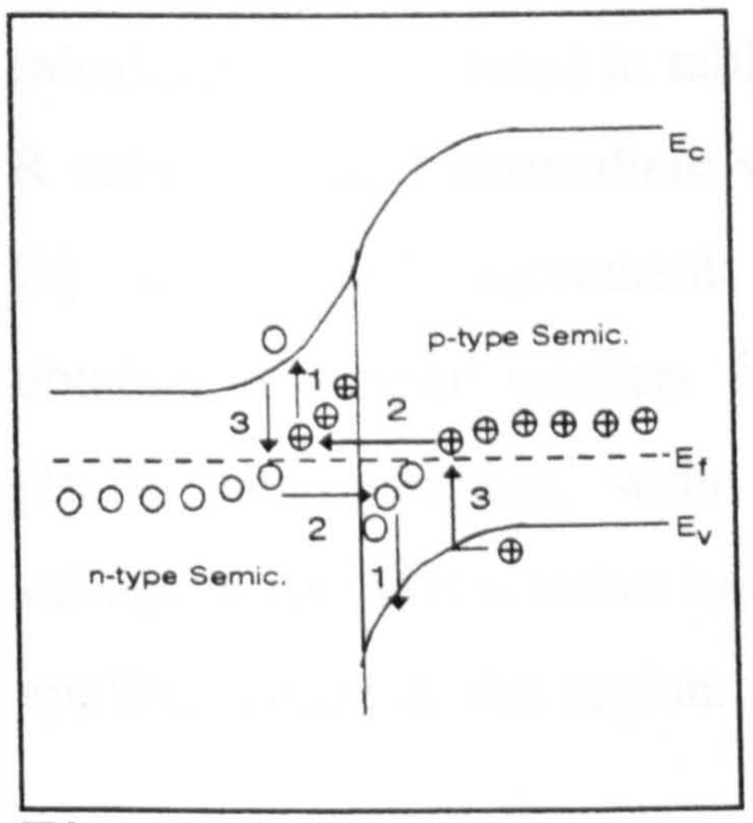

Figure 9.12 .. Possible recombination-trap assisted multistep tunneling process fora p-n heterojunction (step sequences are shown).

$$I_f = \chi N_t \exp[-\alpha R^{-0.5} (V_D - KV)] \quad (9.8)$$

where the temperature dependence of I_o is implicit in V_D, χ is the transmission coefficient of electrons across the junction, N_t is the density of tunneling/recombination centres, R is the number of tunneling steps and:

$$\alpha = (\pi/4h) \sqrt{m_n \epsilon_p / N_A} \quad (9.9)$$

$$K = 1 + (\epsilon_p N_A / \epsilon_n N_D) \quad (9.10)$$

where ε_p, ε_n and N_A, N_D are the dielectric constants and net ionised acceptor and donor densities in the CdTe and CdS respectively, m_n is the electron effective mass and h is the reduced Planck constant. From the average slopes at lower

temperatures (i.e. A′ for T<250K) of the $Ln(I_f)$-V characteristics and taking K=1.5 ($N_A < N_D$, $\varepsilon_p \propto \varepsilon_n$), average R values were calculated and are listed in table IX.III. The R value for the intermediate voltage range (b) is in good agreement with values obtained by other workers for the same [15,19] heterojunction, while in the low voltage range (a) it is rather lower than expected; this might be related to the low applied voltage in this region.

Table IX.III .. Analytical results associated with multi-step tunneling in regions (a) and (b) of figure 9.9 at lower temperatures.

V range	A′	R
(a)	27.5	7
(b)	11	41

9.4. Photovoltaic behaviour of the CdS/CdTe:P solar cell

9.4.1. Illuminated I-V

The photovoltaic I-V output characteristic, for the cell was measured under AM1 illumination at 25°C, and is shown in figure 9.13. The values of V_{oc}, I_{sc}, and FF were 0.7V, 1.83×10^{-4}A, and 37%. Using the unmasked illuminated area of 0.63 mm^2, leads to a short circuit density of 29 $mAcm^{-2}$, which corresponds to an efficiency of 9.4%. The device has a relatively high light conversion efficiency, in spite of its low fill factor. A feature of the fabrication procedure (i.e. slight polishing method, section 8.7) is that it creates devices with doping profiles on both sides of the substrate, yielding a good rectifying junction with the CdS and a good ohmic contact at the back face. The high doping concentration at the back surface has led to a tunnelling ohmic contact with a low voltage drop across it, while at the CdS/CdTe interface, the higher carrier concentration was believed to be the responsible for the high measured open circuit voltage. However, the low fill factor gives a clear indication that the bulk substrate was still too resistive.

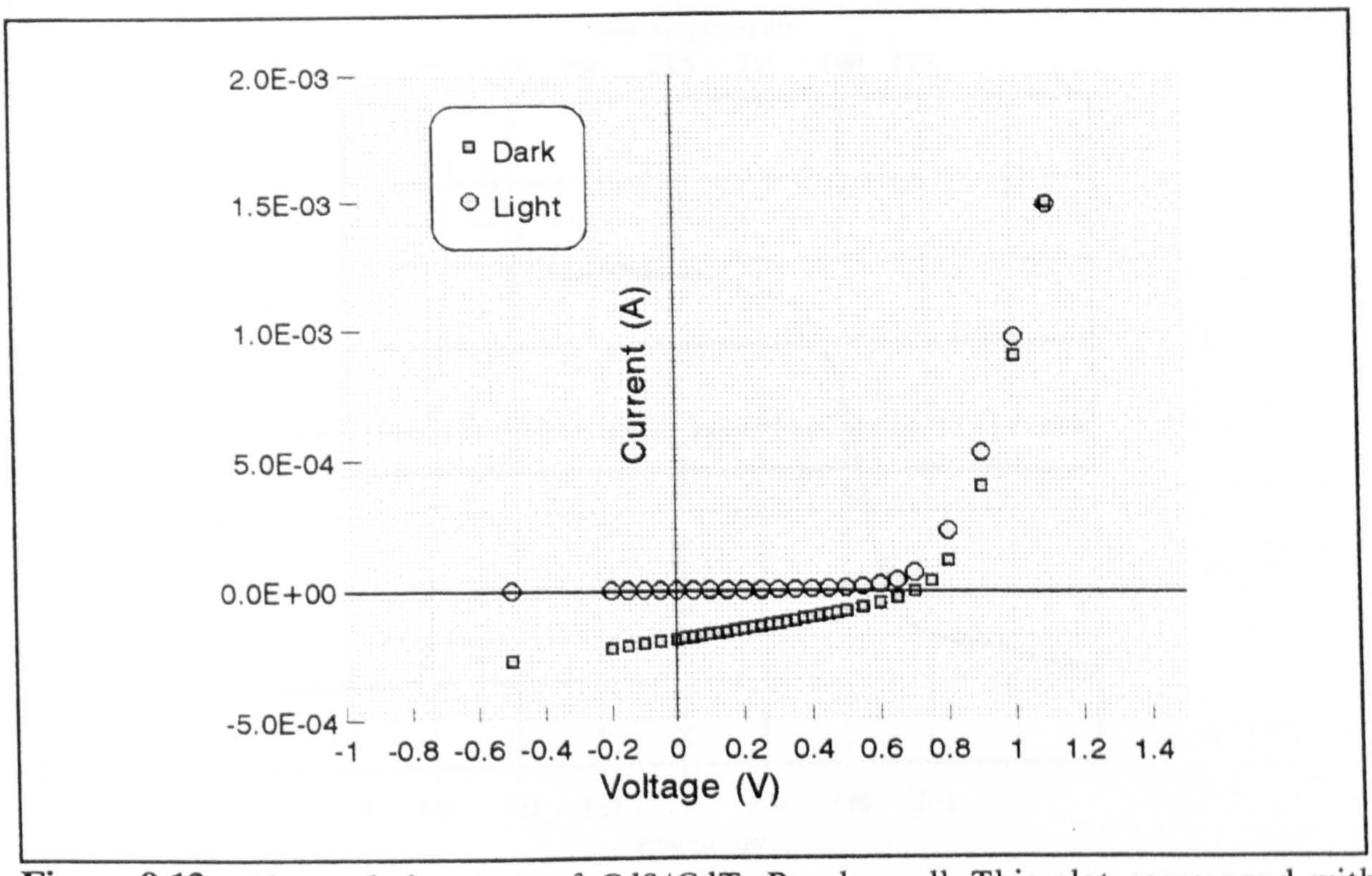

Figure 9.13 .. Photovoltaic output of CdS/CdTe:P solar cell. This plot correspond with the dark I-V characteristics shown in figure1.

9.4.2. Photo-Response

When light is incident on a heterojunction from the high energy-gap side, photons with energies between the two energy gaps, pass freely through the wide-gap material and are absorbed very near the junction in the low energy-gap side. In the case of CdS/CdTe photovoltaic cell, it is expected that photons of energy between 2.5 eV and 1.5 eV pass through the CdS window and create electron-hole pairs at the interface with the CdTe. This is known as the window effect in heterojunctions. Photons with higher energies are absorbed in the window layer before reaching the junction and so do not contribute to the photovoltaic effect in the p-n junction, and, obviously, photons of lower energies are not absorbed in either semiconductor.

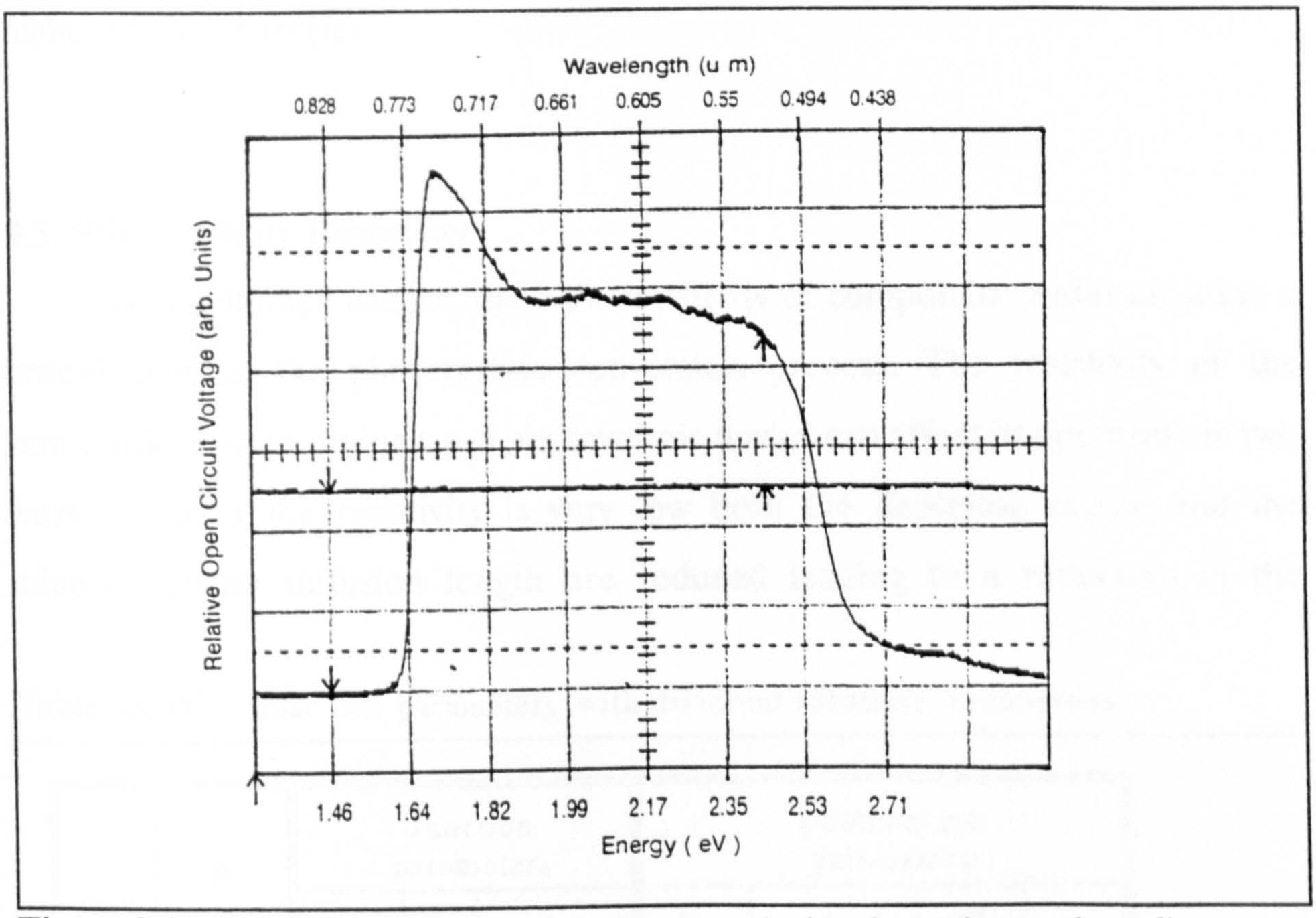

Figure 9.14 .. V_{oc} spectral response of the same device shown in previous figures.

The V_{oc} spectral response for the solar cell was measured at room temperature and is shown together with the lamp response in figure 9.14. The charge carriers that establish the photovoltaic effect across the p-n junction are generated mainly by absorption in the CdTe, and the direct transitions in CdTe are expected to dominate the spectrum. The band gap of CdTe is ~1.5 eV [6] at room temperature and thus the peak at about 1.5 eV corresponds to the energy gap of CdTe. On the other hand, the band gap of CdS is ~2.5 eV [7] and hence the sudden fall of the voltage at 2.4 eV corresponds to absorption in the CdS rather than at the junction itself. The apparent lack of any response at higher energy also suggests that there is little or no space charge in the CdS, indicating a one-sided junction. If this were not the case (i.e. not a one sided junction), then the field associated with the space charge would separate photogenerated electron-hole pairs in the CdS leading to a contribution to the photoresponse at

higher photon energies.

9.5. Effect of Bulk Resistivity

As mentioned earlier, the bulk resistivity of component materials plays a crucial part in the photovoltaic conversion process. The resistivity of the semiconductor(s) forming a p-n photovoltaic device can affect its operation in two ways; firstly, if the resistivity is very low both the depletion region and the minority carrier diffusion length are reduced leading to a reduction in the

Table IX.IV .. Solar cell parameters with different substrate resistivities.

Dev.	ρ (Ωcm)	Junction parameters			photovoltaic parameters			
		Rec.	n	I_o (A)	V_{oc} (V)	I_{sc} (A)	FF (%)	η (%)
a	50	603	2	$5.1x10^{-8}$	0.53	$1.7x10^{-4}$	0.40	7.2
b	354	508	2	$1.9x10^{-7}$	0.523	$1.43x10^{-4}$	0.30	4.7
c	26400	40	2	$1.0x10^{-6}$	0.51	$1.36x10^{-4}$	0.26	3.7

collection width with a corresponding loss of conversion efficiency, secondly, when the resistivity is very high, the solar cell output power suffers substantial reduction because of the high series resistance of the device. The optimum CdTe resistivity for solar cell applications is thought to be in the range of 1-10 Ωcm [8]. The effect of substrate resistivity on device characteristics was studied using CdTe substrates of a range of different resistivities. The devices were fabricated on phosphorus doped p-CdTe with resistivities of 50 Ωcm, 354 Ωcm, and 26K Ωcm. These devices were designated as a, b, and c respectively. Although, these resistivities are all higher than the optimum, nevertheless, they demonstrate clearly the effects of

high resistivity on device performance. Table IX.IV gives the detailed parameters of these three device.

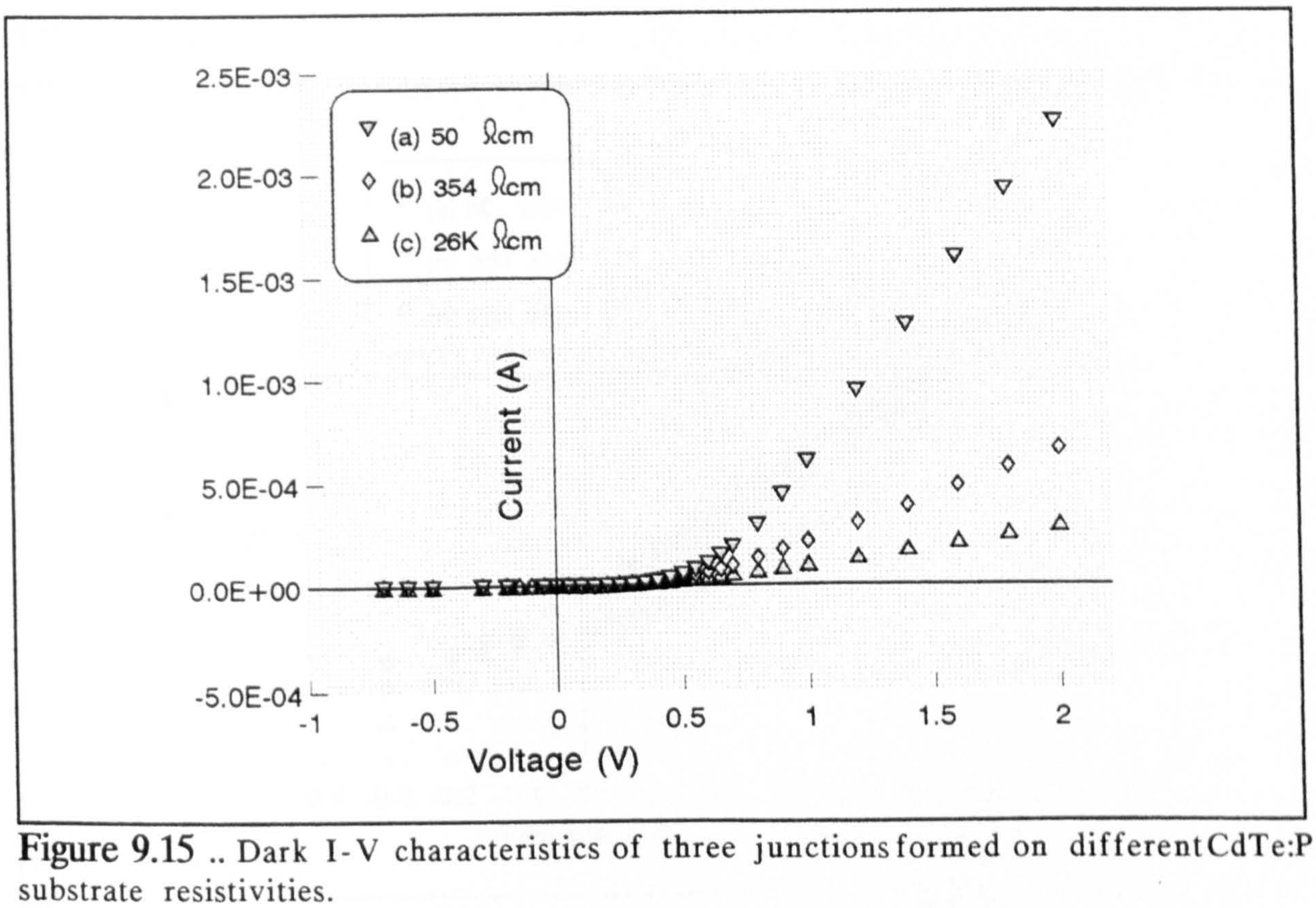

Figure 9.15 .. Dark I-V characteristics of three junctions formed on different CdTe:P substrate resistivities.

Figure 9.15 illustrates the dark I-V characteristics of devices a, b, and c. All devices were rectifying, with rectification ratios of 603, 508, and 40 measured at 0.7 volt for a, b, and c, respectively. The bulk resistivity of CdTe:P substrates has a pronounced influence on the dark output current. As expected, the lower the bulk resistivity, the higher the output current. In spite of that, all the devices displayed ideality factors of ˜2, although there was a progressive increase in the junction leakage current I_o with increasing substrate resistivity. This should have a corresponding influence on the open circuit voltage of the solar cells; where higher values of I_o should lead to lower values of V_{oc}. Open circuit voltage values for the three cells are listed in table IX.IV and showed a small reduction with increasing I_o suggesting that this was not the main factor limiting V_{oc}. Depletion widths, were measured by EBIC, and followed an increasing trend as the

resistivity increased; for the junction based on the 50 Ωcm CdTe the depletion width was 0.8 μm, for the 354 Ωcm device it was 1 μm, and for the 26KΩcm cell it was 1.5 μm.

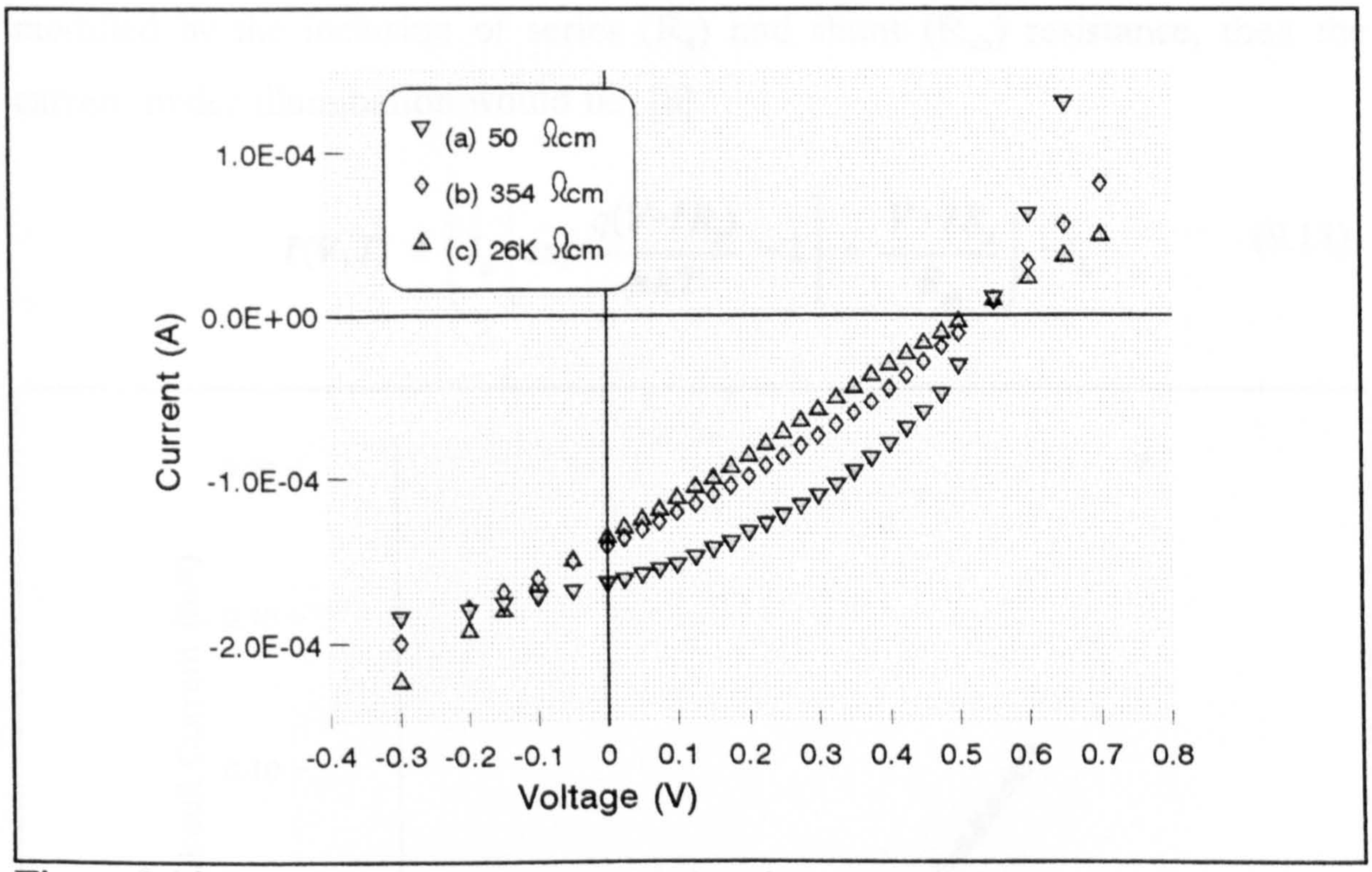

Figure 9.16 .. Photovoltaic I-V characteristics of the three devices.

The photovoltaic output characteristics of the cells measured under AM1 conditions at 25°C are plotted in figure 9.16. Corresponding parameters are given in table IX.IV. Bulk substrate resistivity influenced all the photovoltaic parameters. The most significant effect was on the maximum output power of the devices, with fill factors that varied from 0.25 for the most resistive device to 0.40 for the least resistive one. Both, V_{oc} and I_{sc} increased as the substrate resistivity decreased, although less strongly. Consequently, there was a photovoltaic increase in conversion efficiency with decreasing substrate resistivity.

Although our results are not conclusive in determining the optimum value of the resistivity, they demonstrate the undesirable effect of values for the bulk resistivity that are too high.

9.6. Determination of Device Series and Shunt Resistances

Assuming for the present case that the device current at room temperature could be described by a single space charge recombination diode, which was modified by the inclusion of series (R_s) and shunt (R_{sh}) resistance, then the current under illumination would be; [8]

$$I(V,T) = \left(I_o \left[\exp \frac{q(V+IR_s)}{nkT} - 1 \right] + \frac{V+IR_s}{R_{sh}} \right) - I_L \qquad (9.11)$$

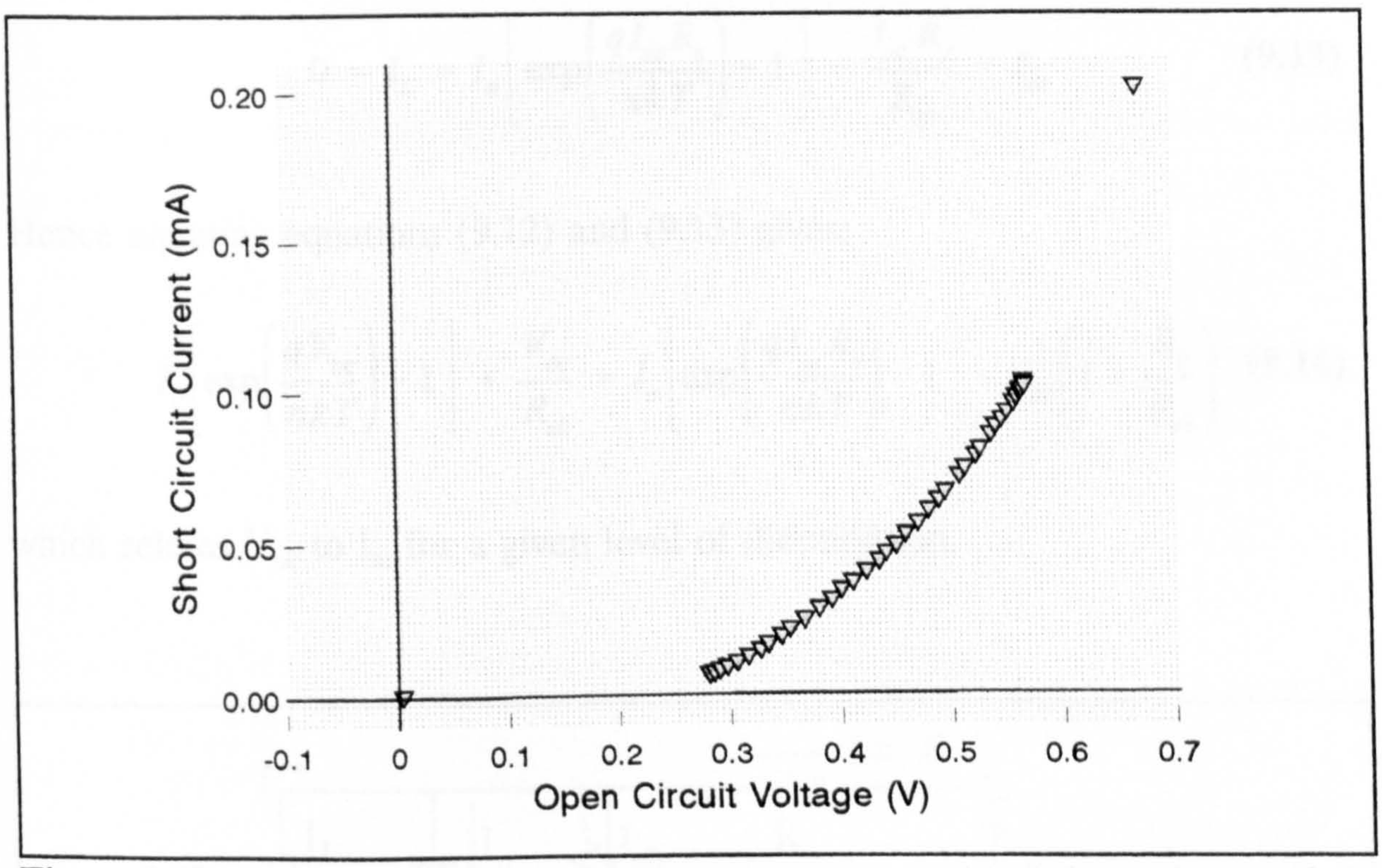

Figure 9.17 ..Variation of I_{sc} with V_{ov} for different intensities of illuminationof the same solar cell.

The series and shunt resistances for a solar cell can be obtained from the variation of V_{oc} and I_{sc} with the level of illumination using equation 9.11. The solar cell was illuminated with variable intensity light and without the use of any external power supply. The measurement consisted of determining the short circuit current I_{sc}, and plotting it against the open circuit voltage V_{oc} for every light intensity setting. An example plot of I_{sc} versus V_{oc} is given in figure 9.17. The equivalent circuits are shown in figure 9.18; where (a) corresponds to the open

circuit condition and (b) corresponds to the short circuit case.

Under open circuit conditions, $V = V_{oc}$, $I = 0$, and equation 9.11 becomes;

$$0 = I_L - I_o\left[\exp\left(\frac{qV_{oc}}{nkT}\right)\right] - \frac{V_{oc}}{R_{sh}} \qquad (9.12)$$

Similarly under short circuit conditions where $V = 0$ and $I = I_{sc}$, equation 9.11 becomes

$$0 = I_L - I_o\left[\exp\left(\frac{qI_{sc}R_s}{nkT}\right) - 1\right] - \frac{I_{sc}R_s}{R_{sh}} - I_{sc} \qquad (9.13)$$

Hence equating equations (9.12) and (9.13) gives;

$$I_o\left[\exp\left(\frac{qV_{oc}}{nkT}\right) - 1\right] + \frac{V_{oc}}{R_{sh}} = I_o\left[\exp\left(\frac{qI_{sc}R_s}{nkT}\right) - 1\right] + I_{sc}\left(1 + \frac{R_s}{R_{sh}}\right) \qquad (9.14)$$

which relates V_{oc} to I_{sc} for a given level of illumination.

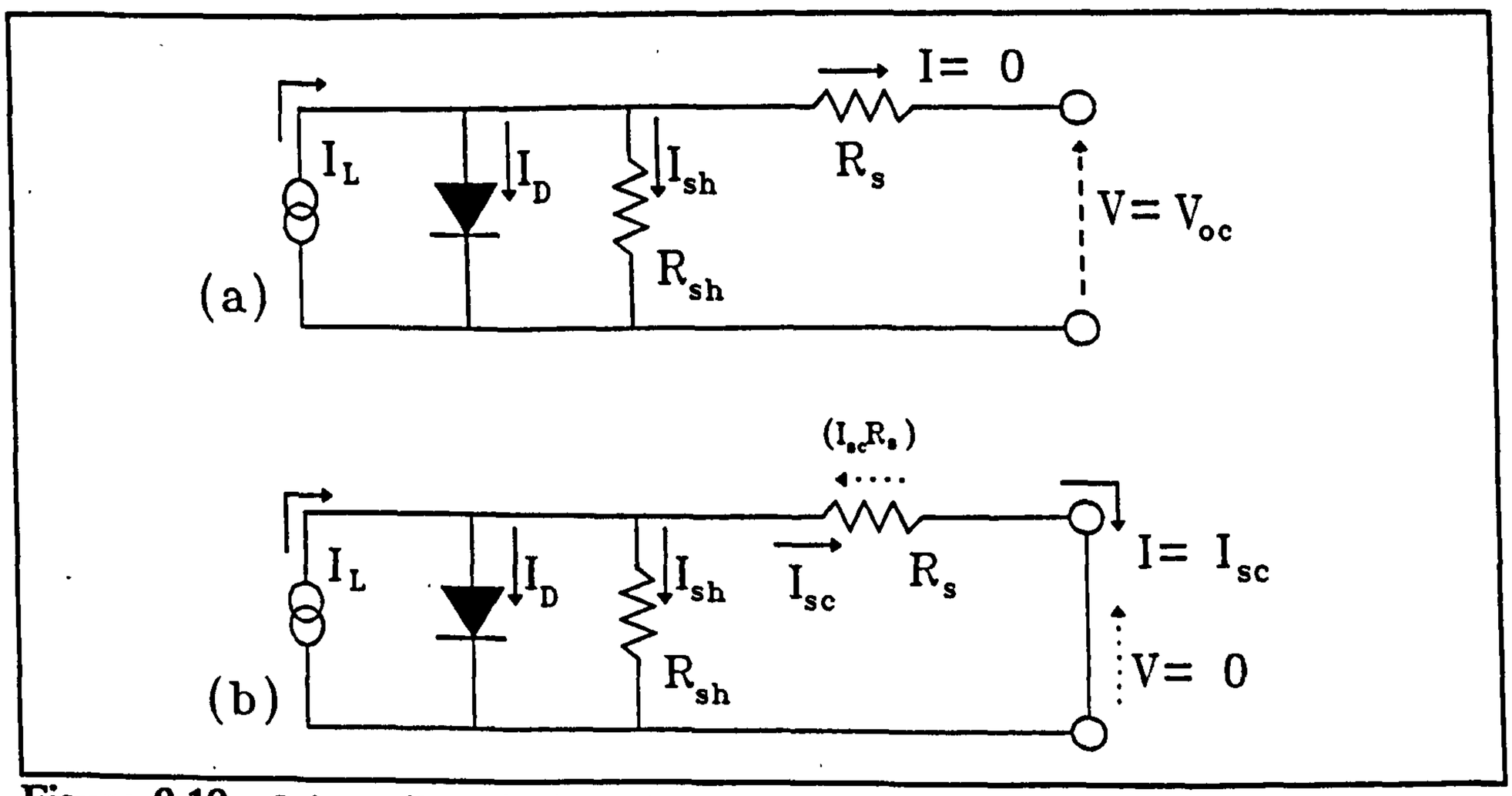

Figure 9.18 .. Solar cell equivalent circuits under illumination in (a) open circuit voltage and (b) short circuit current conditions.

Equation 9.14 cannot be solved analytically since both V_{oc} and I_{sc} appear as the argument of an exponential and as linear terms. Detailed solution would require numerical methods. However consideration of equation 9.14 under high and low levels of illumination does allow approximations to be made and hence estimates to be found for R_s and R_{sh}.

At high levels of illumination (high V_{oc}) the exponential term on LHS of equation 9.14 dominates and the equation becomes;

$$I_o\left[\exp\left(\frac{qV_{oc}}{nkT}\right)-1\right] \simeq I_o\left[\exp\left(\frac{qI_{sc}R_s}{nkT}\right)-1\right]+I_{sc} \qquad (9.15)$$

where it has also been assumed that $R_s << R_{sh}$. Equation 9.15 can then be used to calculate R_s.

Similarly at low illumination levels, (low I_{sc}) the exponential on the RHS of equation 9.14 becomes negligibly small and equation 9.14 is then

$$I_o\left[\exp\left(\frac{qV_{oc}}{nkT}\right)-1\right]+\frac{V_{oc}}{R_{sh}} \simeq I_{sc} \qquad (9.16)$$

(where again $R_s << R_{sh}$) from which R_{sh} may be obtained.

Table IX.V .. Some internal parameters including R_s and R_{sh} of identical CdS/CdTe solar cells made with different back contacts.

Cell	I_o (A)	n	R_s	R_{sh}
UnD-Au	3.8×10^{-8}	1.63	3.8×10^{3}	9.8×10^{5}
UnD-Cu	5.6×10^{-8}	1.09	3.8×10^{3}	4.7×10^{5}
UnD-P	4.1×10^{-8}	1.29	2.3×10^{3}	4.2×10^{5}

Table V lists values of R_s and R_{sh} obtained in this way for three cells, used in the earlier contact study (section 8.5.), where a different method was applied

to determine device series resistance and the results of which were provided in table V of that chapter. R_s values in both tables for each device were comparable, this provides support for the method applied here for the determination of R_s and R_{sh}.

Calculation of the resistances (R_s and R_{sh}) of the cell characterised in figure 9.9, provided average values of device series resistance of 4.3×10^3 Ω and shunt resistance of 3.7×10^7 Ω. As required for a good solar cell, the shunt resistance was many orders of magnitude higher than the series resistance (four orders of magnitude in the present case). Nevertheless, the device was still suffering from high series resistance, and this will have to be greatly reduced if further improvements are to be obtained.

9.7. Discussion and Conclusion

The work described in this chapter was mainly concerned with In-CdS/CdTe:P-P^+-Au heterojunctions formed on bulk single crystal CdTe. Diode internal parameters were determined and charge transport mechanisms proposed. Photovoltaic behaviour was investigated, and finally, the effects of bulk substrate resistivity were studied on device performance.

In spite of the fact that the solar cell performance suffered from high series resistance, and low fill factor, the device achieved a relatively high light conversion efficiency due to reasonably high values of V_{oc} and I_{sc}. High open circuit voltage was believed to be the result of the highly doped interface at the heterojunction. The use of an ultra-thin metallic film onto the window layer was also thought to be a strong contributory factor, as it acts as a good current collector from any where on the active device surface to the top contact. The transmission of such thin In films (on glass) was measured and gave an average value of 75% for the relevant wavelength range of incident light. It is expected

that heat treatments would have a good chance of improving device performance, through diffusion of In into the window layer leading to a considerable reduction in sheet resistance of the undoped CdS and a reduction in top contact resistance. Further improvements could be achieved by optimising material thicknesses, CdTe surface polishing and etching, and junction heat treatment. These devices would have a good chance of providing even better performance, if doped CdS, and thin optimised PGD treated substrates were used.

Measurements of depletion width by EBIC and capacitance-voltage methods (assuming one-sided, abrupt junction) gave values that were of similar magnitude, although not identical. Minority carrier diffusion lengths (from EBIC) in CdTe:P, were rather less than that of untreated material. A previous study [5] reported values for L_n = 2.35 μm in undoped CdTe and L_n = 1.12 μm in CdTe doped with P in a similar way. Starting from identically grown bulk crystal in both studies, higher values of L_n (1.94 μm) in our material indicated there was a lower density of defects probably as the result of better control of the doping process. Obviously, higher values of minority carrier diffusion length lead to higher output currents from the cell when exposed to light.

As was shown in chapter 6, PGD treated CdTe dice had a pronounced increase in doping concentrations at the surface, and so a slight polish and etch procedure was used to take advantage of that. This resulted in an acceptor impurity concentration gradient, leading, presumably, in turn to a back surface field (BSF) effect [10]. Hovel [10] has shown that the BSF effect may enhance the I_{sc} and V_{oc} since such cells have a very small recombination velocity at the back contact [11]. Further, the current collection efficiency of the cell may also be significantly improved, if the carrier diffusion is aided by the built-in electric field resulting from dopant concentration gradients [12]. Silicon solar cells containing built-in fields have shown the expected increase in efficiency [10].

Low junction leakage currents I_o, have given rise to relatively high open

circuit voltages V_{oc} indicating good junction formation, and improved junction perfection (compared to previous studies [5]). This was confirmed by the nearly square shape of the spectral response of the device. The charge carriers which establish the photovoltaic effect across the p-n junction were generated mainly by absorption in the CdTe, and the direct transitions in CdTe dominated the spectrum. Both the sharp increase and the decrease in the spectral response correlated well with the band gaps of the two semiconductors involved.

Current transport mechanisms were also studied, it was shown that the current-voltage characteristics displayed three regimes, although, detailed analysis indicated that there were probably two transport mechanisms of importance in

Table IX.VI .. A summary of performance values of an optimised CdS/CdTe solar cell. Measurements used were; ♥; I-V, ♠; C-V, ♦, EBIC, and ♣; estimated.

Photovoltaic parameters ♥			
I_{sc} (A)	V_{oc} (V)	FF (%)	η (%)
$2.1e^{-4}$	0.72	32	9.5

Junction parameters ♥								
D_1		D_1		D_2		V_D♠ (eV)	W_o (μm)	
I_{o1} (A)	n_1	I_{o2} (A)	n_2	I_{o3} (A)	n_3		♠	♦
$4.8e^{-9}$	1.5	$2.7e^{-8}$	4.5	$8.2e^{-9}$	3.5	0.61	0.22	0.9

Materials factors			
L (μm) ♦		P ♠	ρ ♣
n (CdTe)	p (CdS)	(cm^{-3})	(Ωcm)
1.95	0.86	$1.6e^{16}$	50

our devices over the temperature range from 100K to 400K. In particular, there was a change from charge tunneling to space charge recombination at a temperature of 250K. A double diode model was, therefore, introduced. Such behaviour has been reported earlier in the literature. Rohatgi et al [9] and Simmons et al [8] have both reported two transport mechanisms operating within their devices, with a space-charge recombination transport mechanism becoming dominated by a tunneling mechanism as the temperature was reduced below 250 K. It is proposed that band-to-band tunneling is unlikely to take place in our device, since the band gaps are relatively large and doping levels were not degenerate. However, a multi-step tunneling recombination model would explain the observed behaviour [14-16].

Bulk crystal resistivity is a major challenge facing CdS/CdTe solar cells. This was well illustrated in the effect on both current rectification and reverse saturation current in the dark characteristics of bulk resistivity, where high resistance resulted in very poor diode characteristics. Under illumination, higher values of bulk substrate resistivity tended to increase the depletion reigion at the junction and hence the collection width, but would result in reduced values of V_{oc} and fill factor. As a summary, parameters from the best solar cell are given in table IX.VI. Photovoltaic parameters for the typical samples varied with values of V_{oc} from 0.53 to 0.74 V, J_{sc} from 18 to 22 mA/cm^2, and FF from 39 to 41.7 %, which gave efficiencies ranging from 4.37 % to 9.4 %.

9.8. References

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Chapter X

Summary and Conclusion

The aim of the work reported in this thesis was to investigate the photovoltaic properties of CdS/CdTe solar cells based on post-growth doped (PGD) single crystal CdTe substrates. Two PGD methods were optimised to achieve a p-type material with a resistivity of 2 Ωcm with a carrier concentration of 5.5×10^{16} cm^{-3}. Considerable progress was also made with the p-CdTe ohmic contacting problem. As a result it was then possible to prepare 9.5 % efficient solar cells.

Post-growth doping of CdTe involves a two stage process. In the first stage a thin layer of a mixture of Cd_3P_2+P in various proportions, is deposited on the sample surface. During the process, acceptor impurities are presumably incorporated into the CdTe by in-diffusion from the doping layer. Annealing, as a second stage, in Te activates the dopant and probably adjusts the stoichiometry of the CdTe matrix by introducing cadmium vacancies. The optimum treatment for producing good conductive p-type CdTe crystals was found to be: 1) heating in saturated H_3PO_4 vapour at 550 °C for 4 days using the 'open tube' method, and then, 2) annealing in Te vapour at 400 °C for 5 days. Better results were achieved using a fresh system for each row and a continuous saturated flow of acid vapour. However, this may be carried out by using containers other than silica tubes, which should withstand the H_3PO_4 attack, and using thermally insulating tape wrapped round external tubes to ensure a low temperature gradient throughout the system to prevent the vapour path being blocked by acid condensation.

Although orthophosphoric acid is less dangerous and cheaper than other P source materials it should only be used in the open tube method. Further modifications to the system could be useful, for example by using a double zone furnace. It was inferred that annealing in Cd or Te vapour after treatment in H_3PO_4 vapour influenced the conductivity by changing the intrinsic vacancy concentration rather than by influencing the phosphorus site occupancy. In this way annealing in Te introduced additional acceptors (or reduced the concentration of compensating donors) contributing to p-type conductivity, while annealing in Cd introduced donors compensating the conductivity due to phosphorus-related acceptors. It was found that temperature fluctuations and the thermal gradient in the annealing furnace played a crucial role in the success of the process. Further investigation of these effects should prove rewarding.

Although, C-V carrier concentration depth profiling showed that an extended treatment in H_3PO_4 facilitates the uniform diffusion of phosphorus into the bulk, it is advisable to re-examine such a doping profile using more accurate methods, such as Auger or SIMS. Such measurements would also give better estimates of the overall dice carrier concentration rather than Atomic Absorption which has greater limitations for P atoms in such relatively low concentrations. Cathodoluminescence microscopy indicated that the PGD process was assisted by pipe diffusion, and, TEM analysis has provided excellent intimation for ohmic contact formation.

In addition to confirming that the material was p-type, In/CdTe Schottky diodes provided another route to estimate the carrier concentration, as well as a measurement of the depletion width. It was helpful, also in the investigation of different types of ohmic contact material and tests of substrate resistance. The

In/CdTe junctions were characterised using I-V, C-V and EBIC measurements at various temperatures. In spite of the low measured barrier height, diodes showed obvious Schottky junction behaviour. The problems of bulk resistivity and ohmic back contacts are well on the way to being solved in p-CdTe based junctions. Such devices have shown that PGD CdTe would be suitable for the fabrication of solar cells.

In most of the reviewed literature, it was apparent that, ohmic contacts to p-CdTe are most successful when a p^+ layer is introduced at the interface with an electronegative metal or compound. Such an approach fulfills the objective of achieving tunneling type ohmic contacts to CdTe:P. In this way, several contacting procedures were applied to otherwise identical cells, this involved Sb, Cu, Au, P, and Graphite. P gave relatively good results compared with the other investigated materials. As a result, further investigations were performed to optimise the deposition and annealing conditions. Even so, further examination is needed to optimise the other contact materials as some of them such as Cu and graphite are very promising. Several methods of applying phosphorus were studied. These indicated that further success is most likely to be obtained by using thin (<1 mm) PGD CdTe and removing the highly damaged part of the surface with a slight polish, to retain the {111} orientation. Then high values of V_{oc} and I_{sc} should be achieved, and even higher fill factors might result. We expect this method to provide competitive conversion efficiencies. Of course, the stability of these devices remains to be investigated.

As a superior mode of ohmic contact formation to p-CdTe:P, heavily doped surfaces were utilised in ohmic contact and heterojunction formations. The

resulting devices were of the form of In-CdS/P^+-CdTe-P^+-Au. The internal diode parameters were identified and a mechanism of charge transport was proposed. The photovoltaic behaviour was studied, and finally, the bulk resistivity of the substrate was investigated to determine its effect on device performance.

Although the performance of our solar cells has suffered from high series resistance, as evidenced by a low fill factor, a high conversion efficiency was achieved. This was due to the high values of V_{oc} and I_{sc}. The high open circuit voltage was thought to be the result of the highly doped interface at the heterojunction. The high I_{sc} probably reflects the reduced bulk resistivity, good back contact, and the beneficial role of the ultra thin metallic coating on the window layer. This last metallic layer plays an interesting part in device output power. In spite of its effects on transmission, it may be used to reduce the sheet resistance of the undoped CdS window layer. This can be done by applying heat treatment to this thin In layer, which decreases the top contact resistance by diffusion into the window layer. Other improvements could be made by optimising material thicknesses, the CdTe surface polish and etchant, and junction heat treatment. Devices would have a good chance of giving even better performance if doped CdS, and thin optimised PGD treated substrates were used.

With this abrupt junction, the depletion widths measured by EBIC microscopy correlate reasonably with those calculated from C-V measurements, although, interface states are thought to be behind the increase in junction capacitance. The minority carrier diffusion length in CdTe:P, is rather less than that in untreated material. Minority carrier diffusion lengths in undoped CdTe are about L_n = 2.35 μm, while our PGD treated material gave L_n of about 1.94 μm, indicating little disturbance to the semiconductor lattice. This together with the better control of the doping process, leads to the conclusion that success has been

achieved in optimising the PGD process for CdTe using P as the dopant. As was shown from the TEM studies the PGD treated CdTe dice have pronounced higher doping concentrations at the very surface. A slight polish and etch would not be expected to eliminate this high concentration completely. This could result in a pronounced acceptor impurity concentration gradient, leading in turn to a back surface field (BSF) effect which could have led to the enhancement of I_{sc} and V_{oc}. Both the suitability of the semiconductors involved and the junction perfection was confirmed by the nearly square shape of the photoresponse. Where the long and short wavelengths thresholds in the spectral response correlate well with the band gaps of the two semiconductors.

The current transport mechanism has been explored extensively. Two regimes seem to be involved as the process shifted from a charge tunneling dominated mode to a space charge recombination one. This two phase mechanism change was seen at 250 K, before which a tunneling process is dominant and after which a space charge recombination mechanism takes over. In the tunneling regime, a multi-step process was thought to be more appropriate and the number of tunneling steps was calculated. A double diode model has been proposed.Bulk crystal resistivity is still a major challenge facing CdS/CdTe solar cells. This is demonstrated by both the current rectification and the maximum output power obtained.The measurement of the depletion region supported this conclusion, since the depletion width increased as the resistivity of the CdTe increased. Such an increase had the effect of decreasing both V_{oc} and FF, but surprisingly not I_{sc}. Most obviously, as the bulk resistivity was reduced the fill factor of the photovoltaic characteristic increased and with it the light conversion efficiency. A summary of results from the best solar cell produced is recorded in table VI of chapter 9.